NAND Flash Design for 30% Power Reduction

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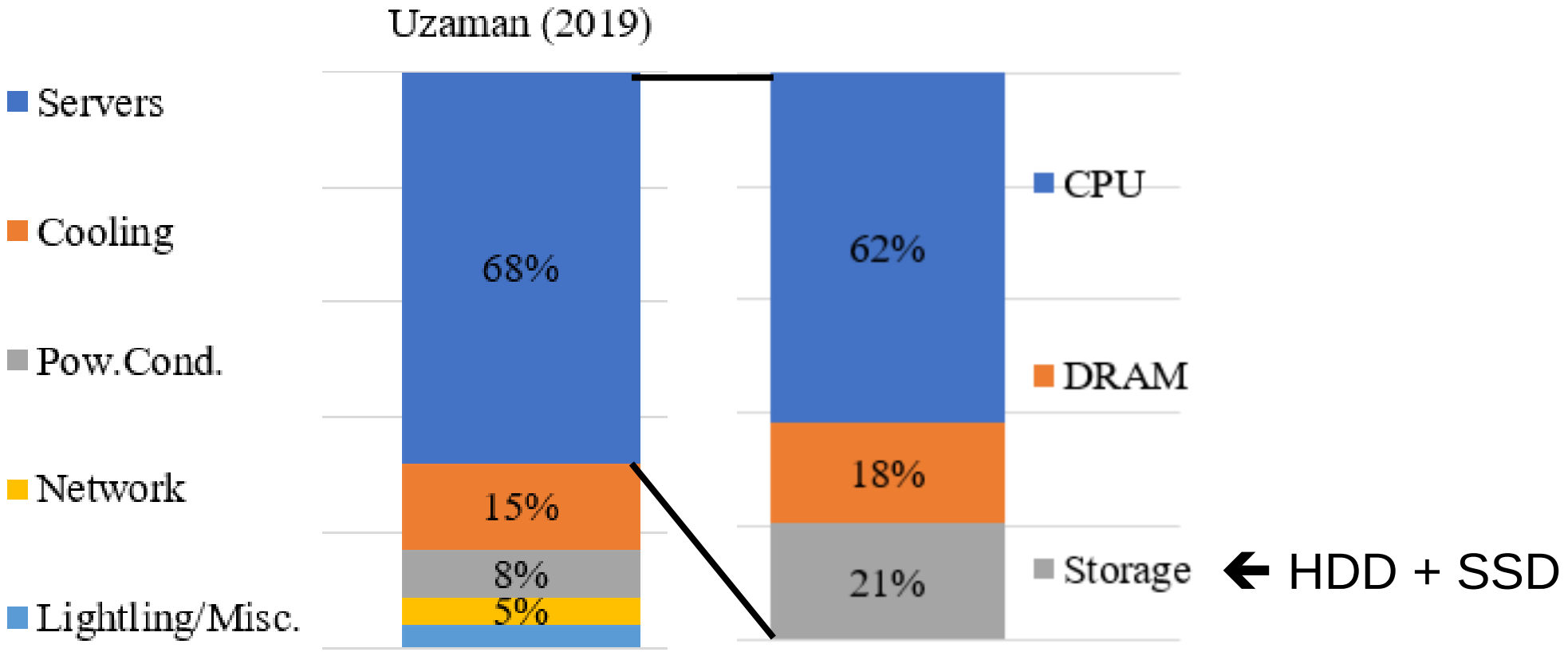
the Future of Memory and Storage

Contributing to a greener society
through innovative researches on integrated circuit design

Power breakdowns for data center

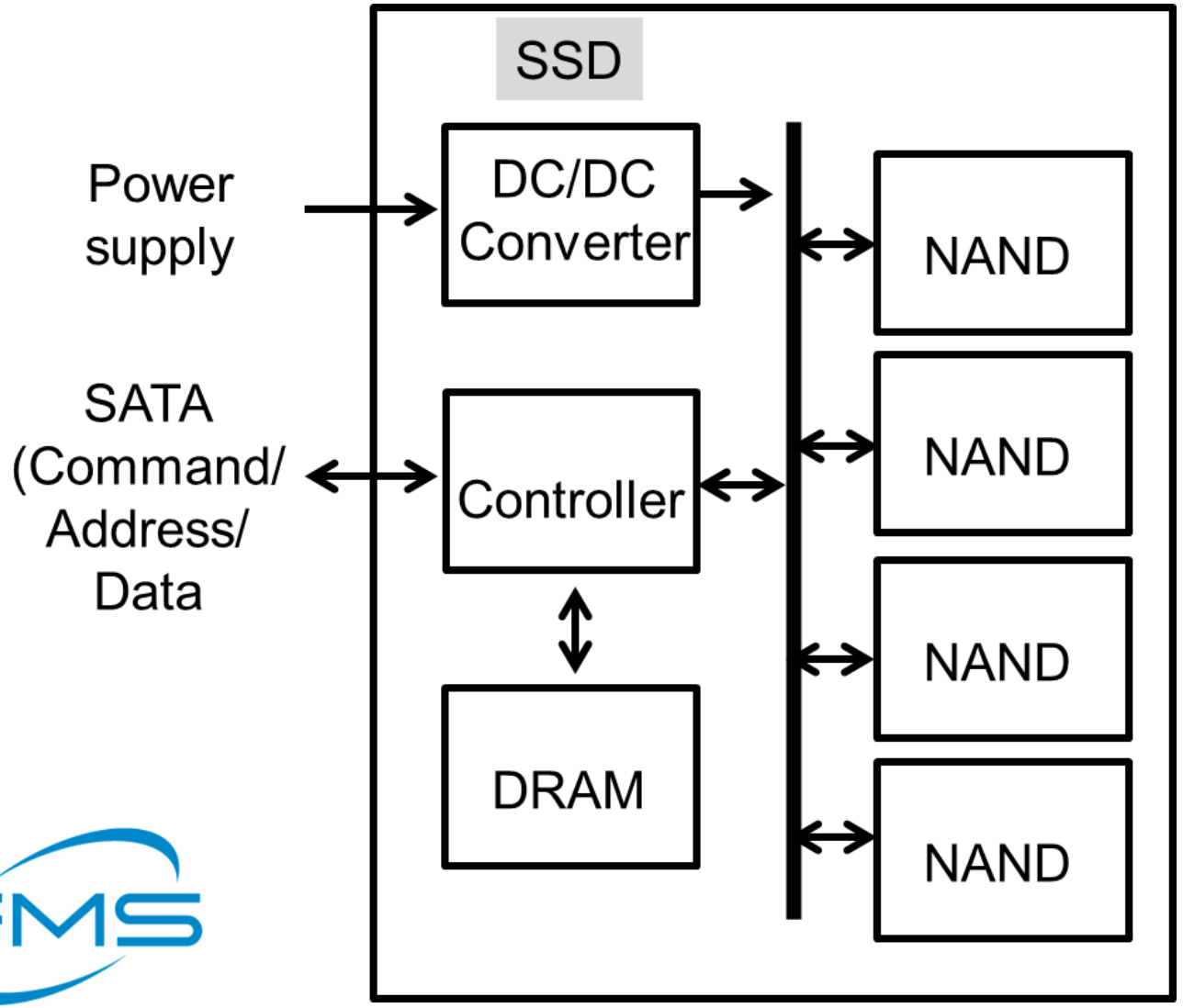
- “Data centers consumed about 460 TWh of electricity worldwide in 2022, almost 2% of total global electricity demand.” (International energy agency, 2024)
- “Global data center electricity use to double by 2026” (Data Centre Dynamics Ltd)



Storage devices consumes 68% X 21% ~ 14% of power in datacenter.

Internal structure of an SSD

M550 M.2 Type 2280 NAND Flash SSD

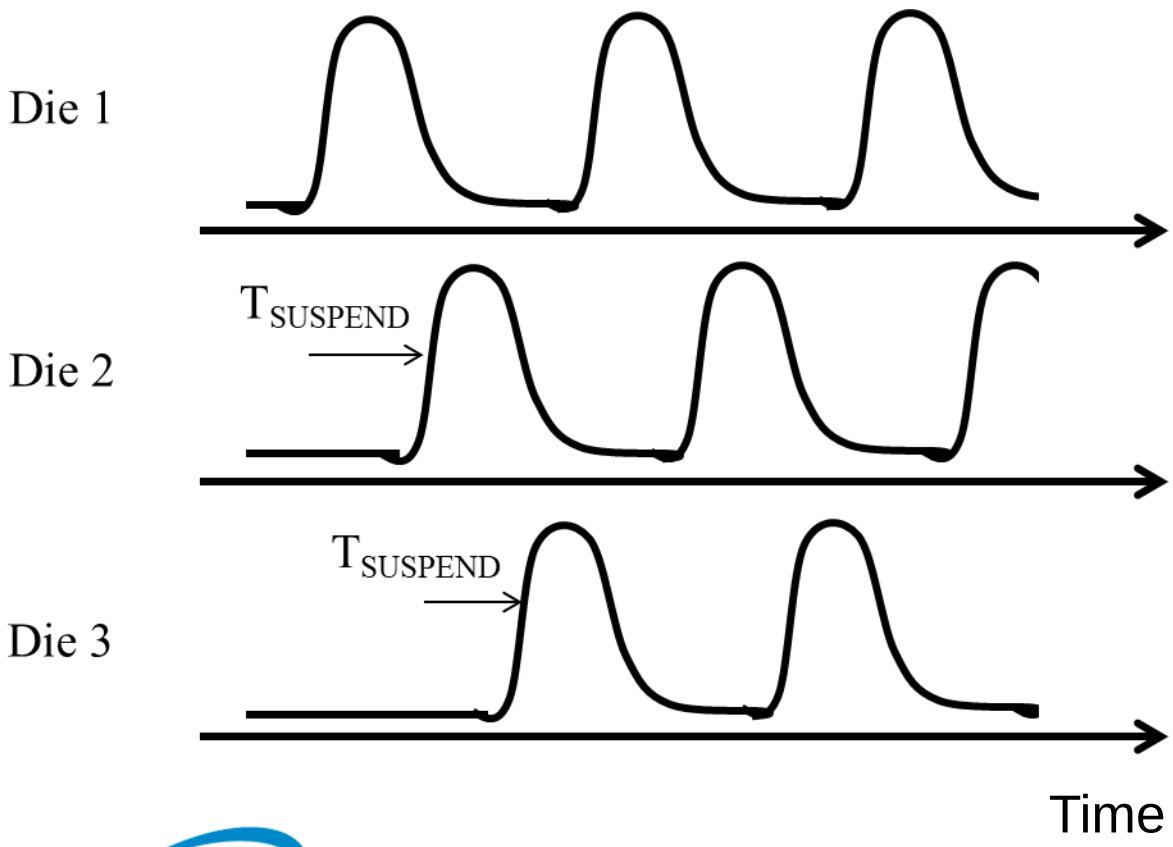


- Multiple NAND dies in SSD
- 3V and 1.2V power supplies for NAND

Aim: Power reduction without impacting die size and read latency while maintaining compatibility with the existing NAND interface.

Existing low power NAND design

Power profile (Siau, ISSCC, 2019)



(Issue) Peak power limits the number NAND dies operating simultaneously.

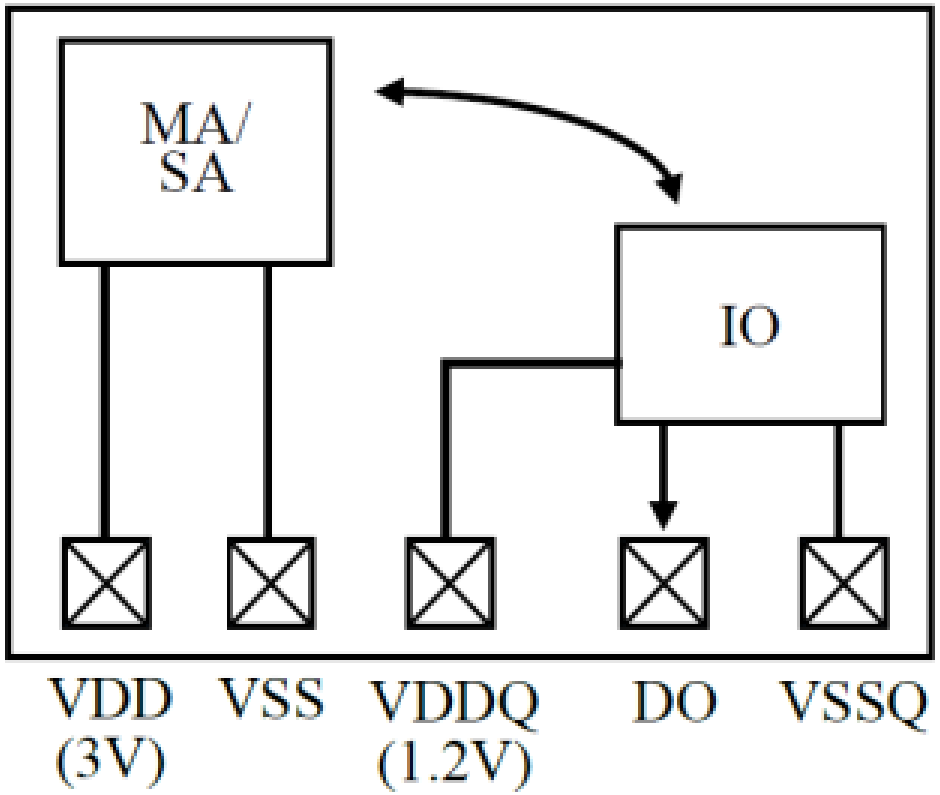
(Solution) Shift the peak power points.

(Drawback) Decrease in throughput due to longer average cycle time.

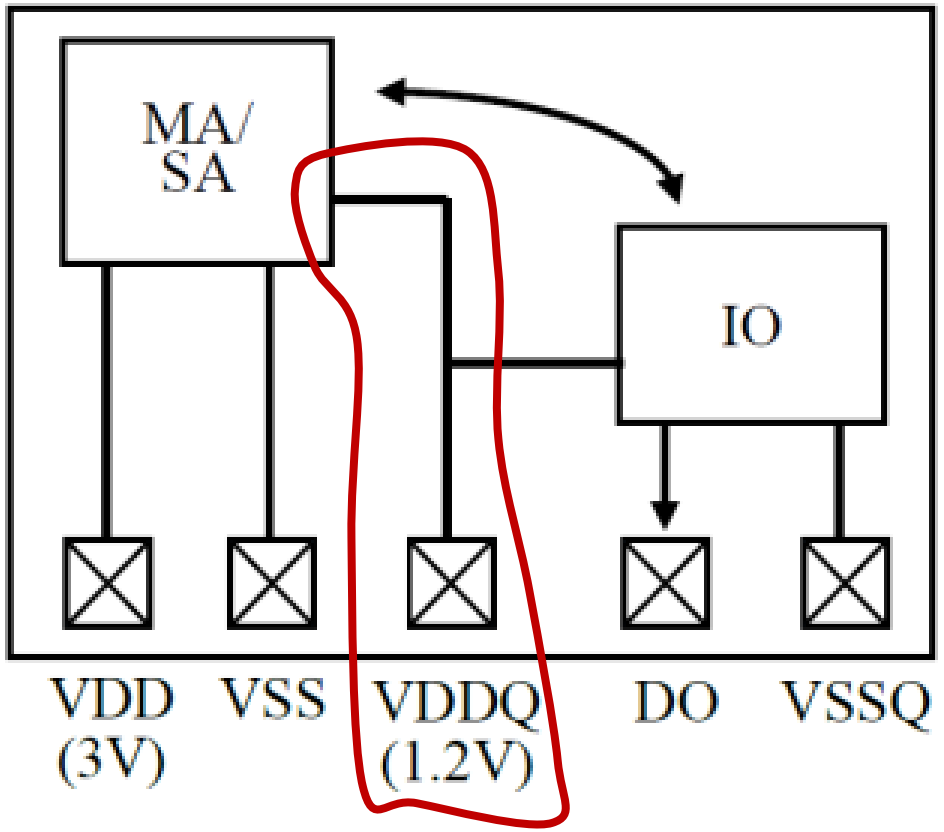
Power distribution for NAND die

ONFI,
https://www.onfi.org/

ONFI 4.0



Proposed

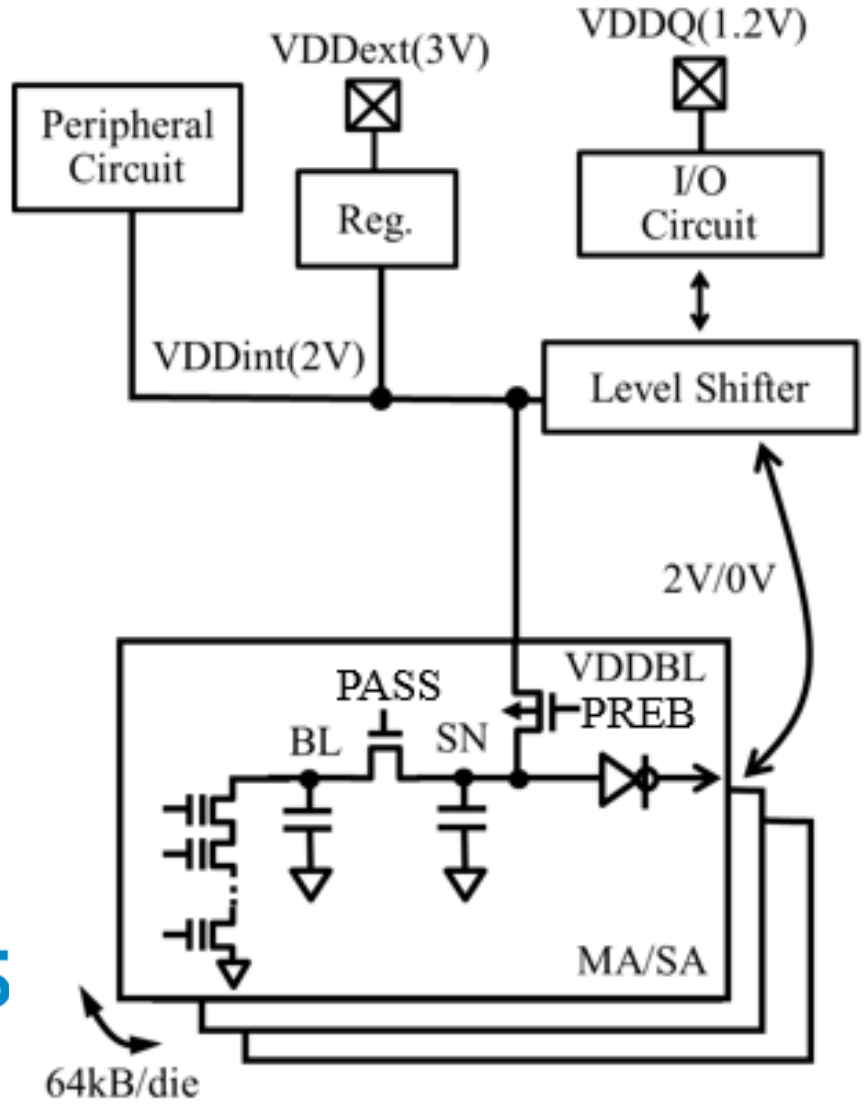


- 1.2V VDDQ used for pre-charge operation for power reduction
- Existing NAND interface available

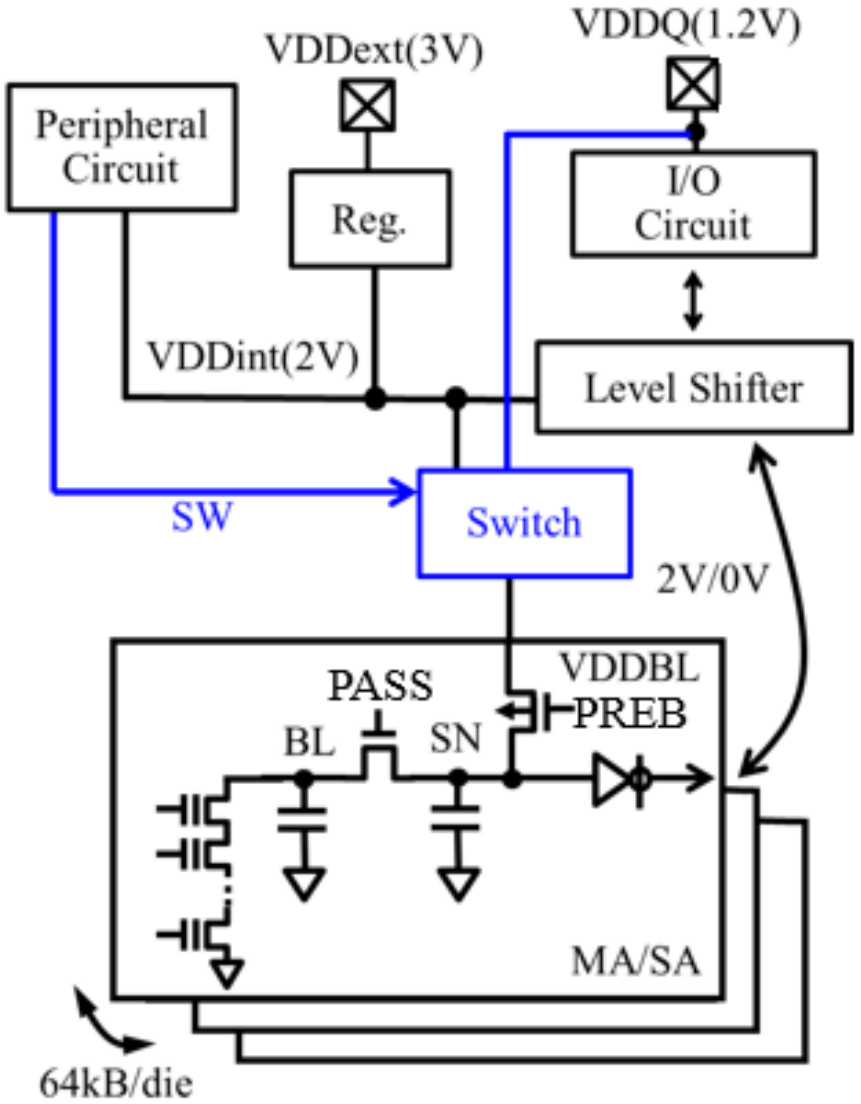
Inside NAND die

Power reduction: 30%
Overhead: Die size < 0.1%, Latency ~ 2%

Conventional

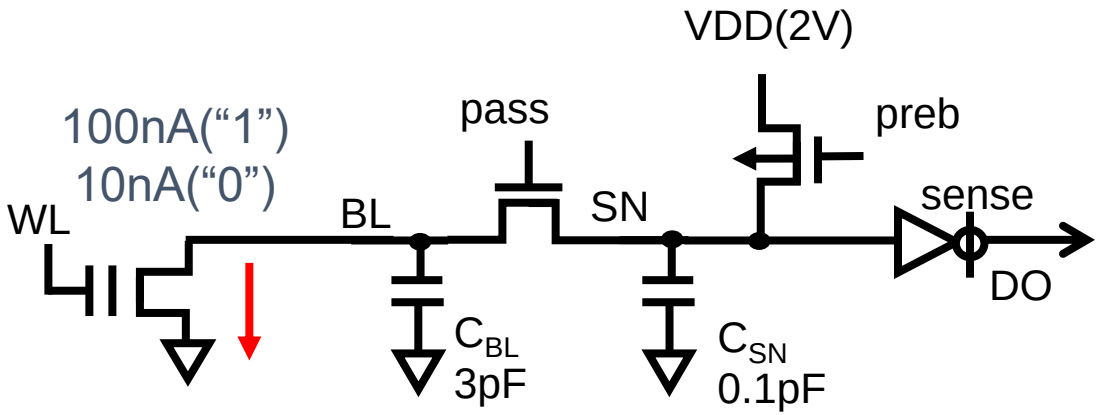


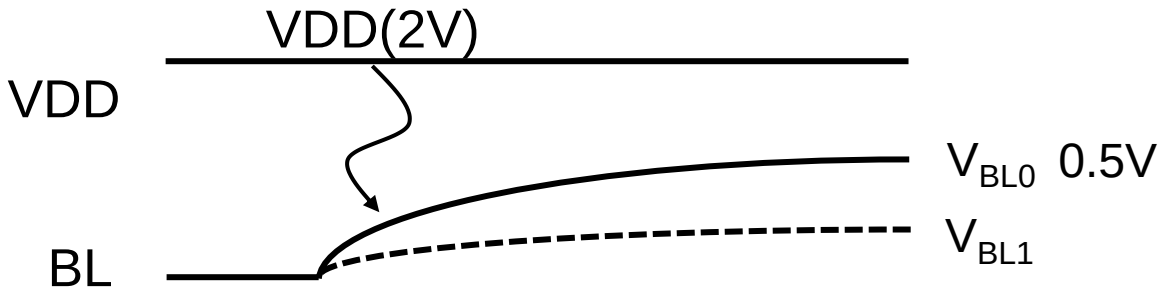
Proposed



BL pre-charge operation

Conventional



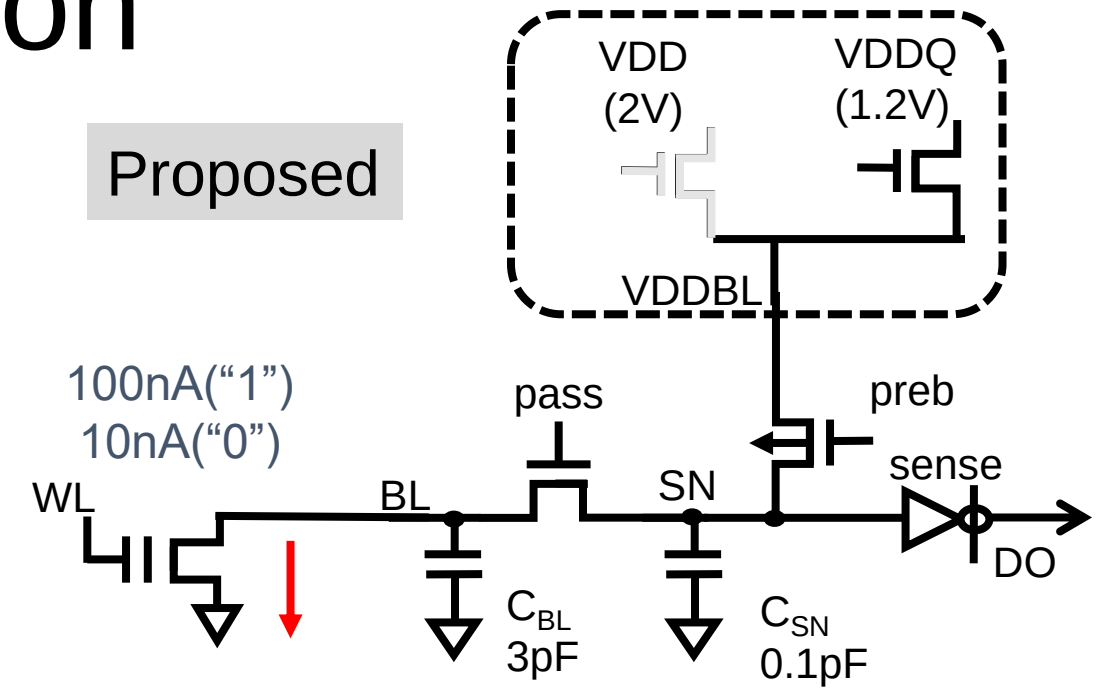


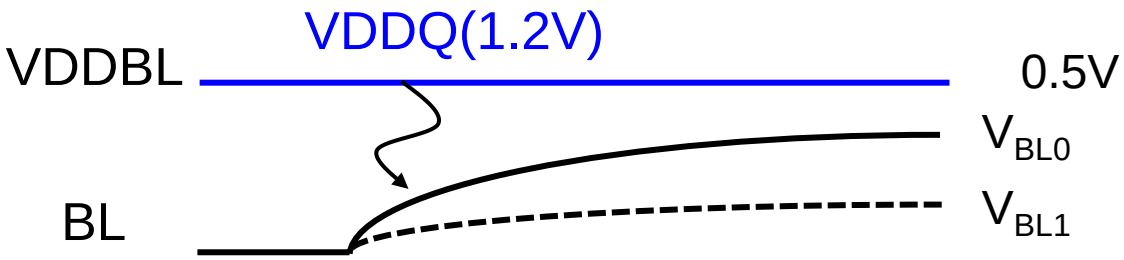
$C\ V_{BL}\ V_{dd}$ $(3pF \times 0.5V + 0.1pF \times 1.6V) \times \underline{3V}$

$I_{cell}\ T_{BL}\ V_{dd}$ $100nA \times 5.0us \times \underline{3V}$

6.3pJ

Proposed





$(3pF \times 0.5V + 0.1p \times 0.8V) \times \underline{1.2V}$

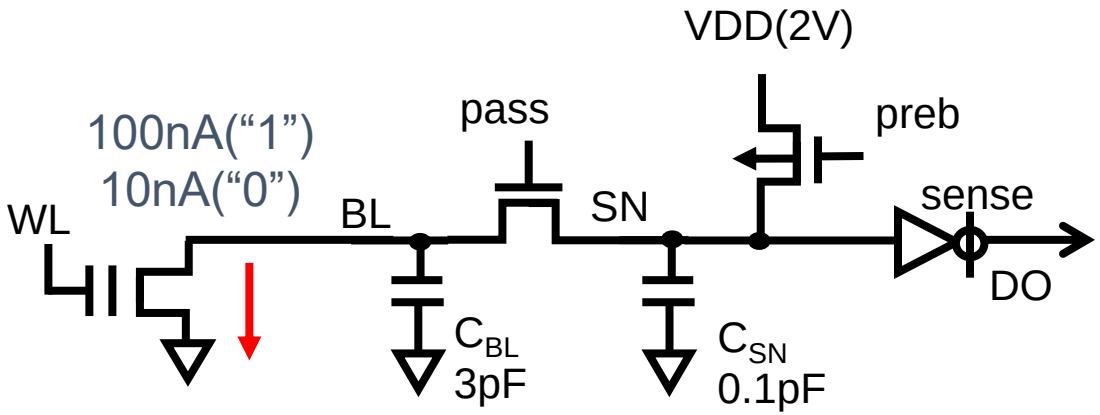
$100nA \times 5.0us \times \underline{1.2V}$

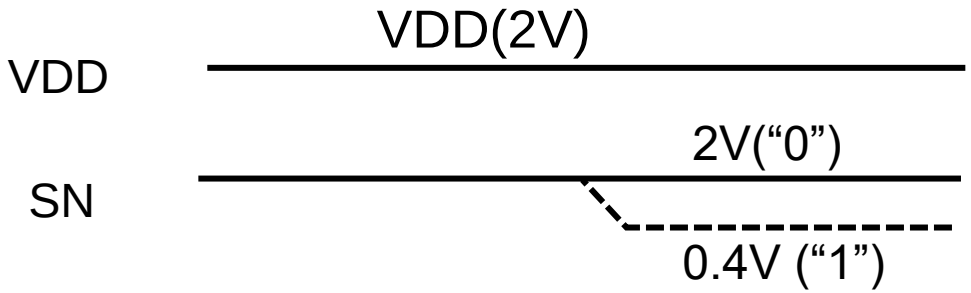
2.5pJ

Power reduction for BL pre-charge

BL sensing operation

Conventional





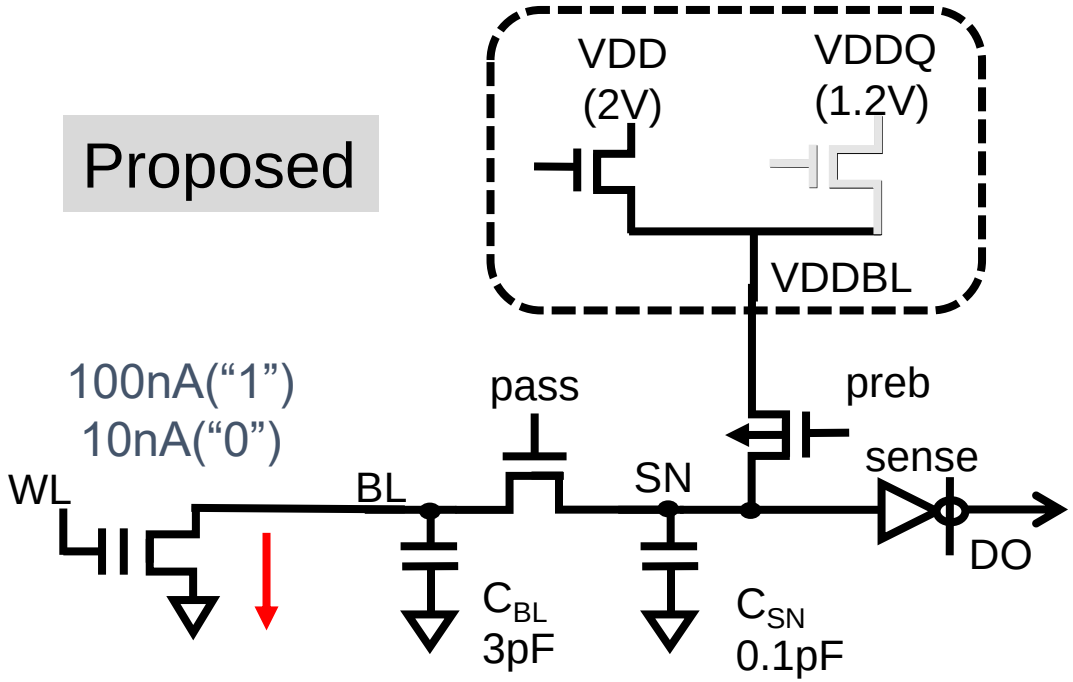
$C_{BL}\ V_{BL}\ V_{dd}$

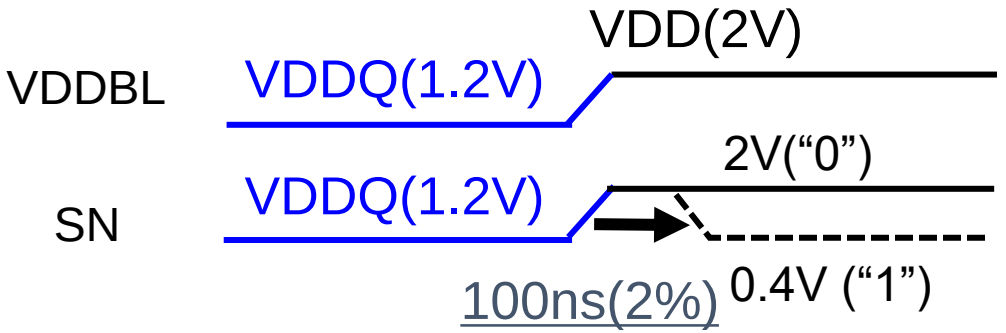
$I_{cell}\ T_{BL}\ V_{dd}$

0 pJ

Power reduction in BL path ~ 60%

Proposed





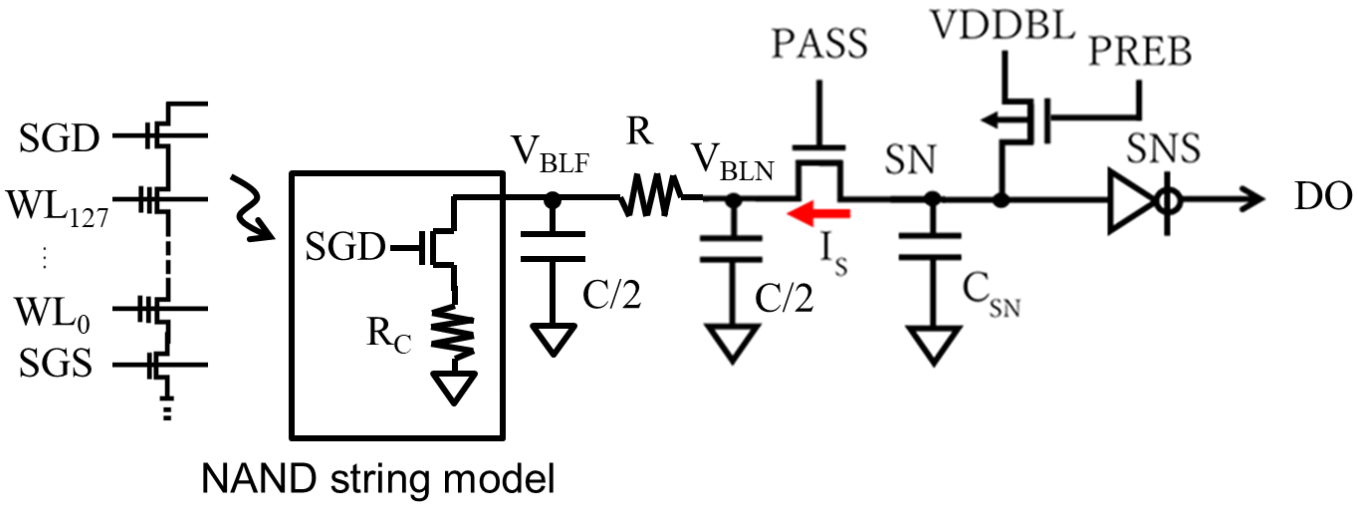
0.1pF × 0.8V × 3V

100nA × 0.1us × 3V

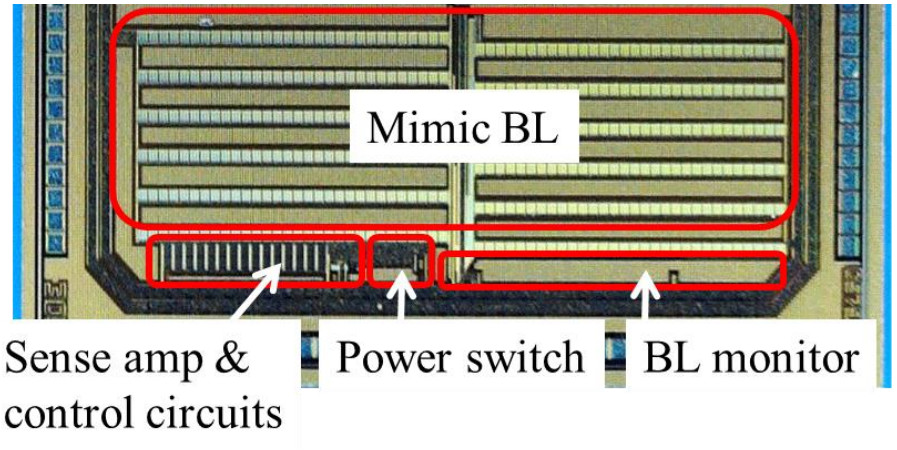
0.3pJ

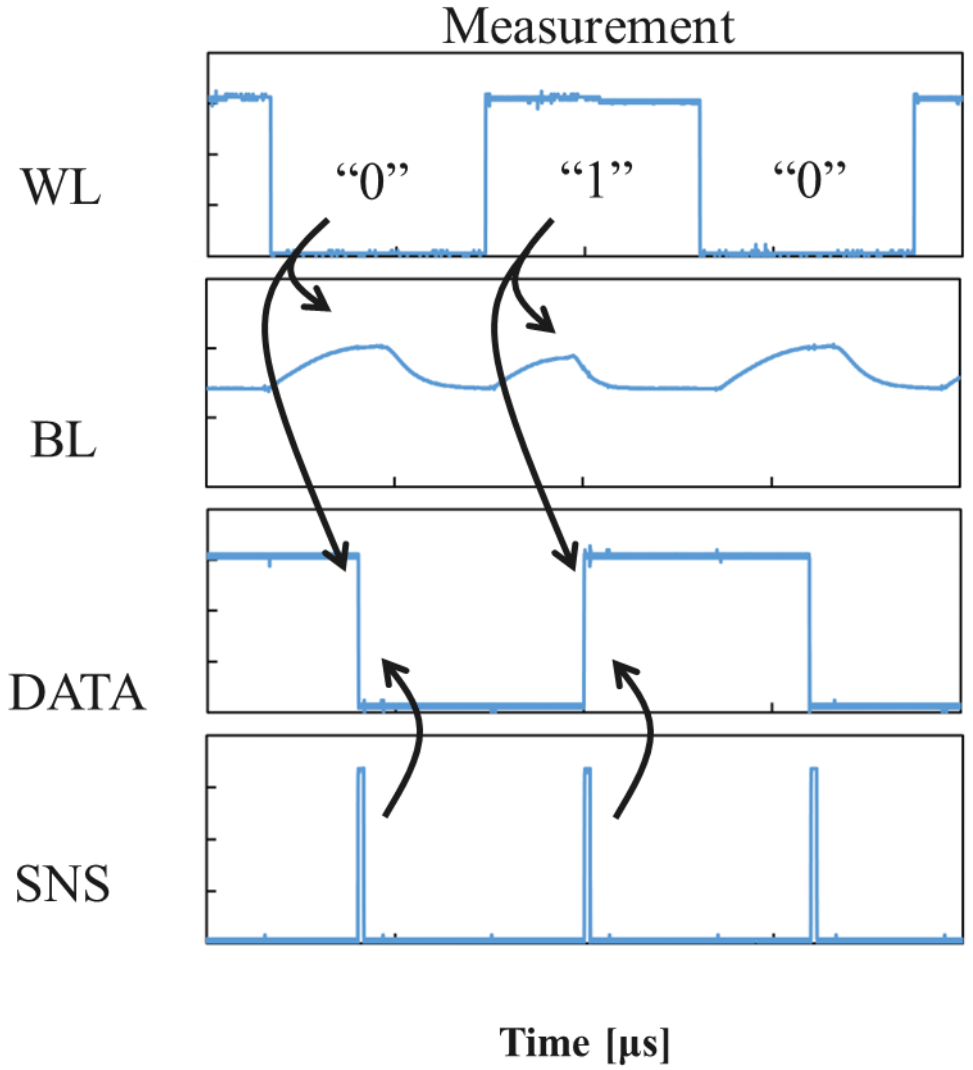
Overhead in read latency ~ 2%

Validation of the proposed design



NAND string model

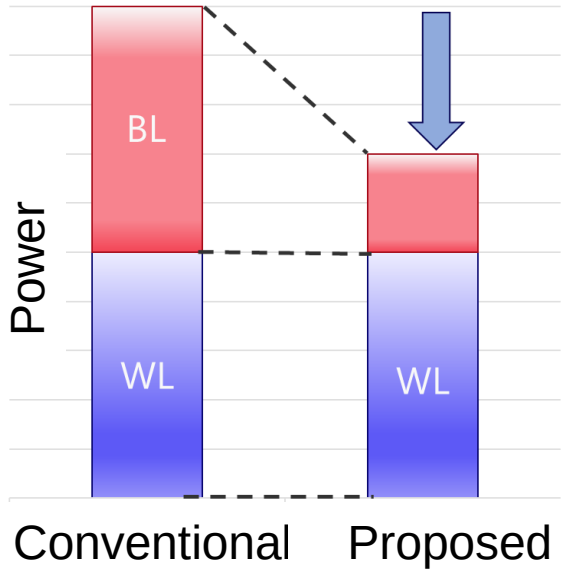




- Standard 180nm CMOS
- MIM-caps and poly-resistors as BL RC

Summary

60% reduction in BL path
~ 30% reduction in NAND die



	Conventional	Proposed
Power supply for BL pre-charging	VDDext (3V)	VDDQ (1.2V)
Power supply for senseamp	VDDint (2V)	VDDint (2V)
Power for read operation	**1 (normalized)**	**0.7**
BL access delay	1 (normalized)	1.02
Die size	1 (normalized)	1.001

- 30% power reduction for NAND while maintaining compatibility with the existing NAND interface
- 4% power reduction for data center
  (30% (per NAND) x 21% (Storage/server) x 68% (Server/data center))

References

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