SSD Challenges in Low-Earth-Orbit (LEO) Applications

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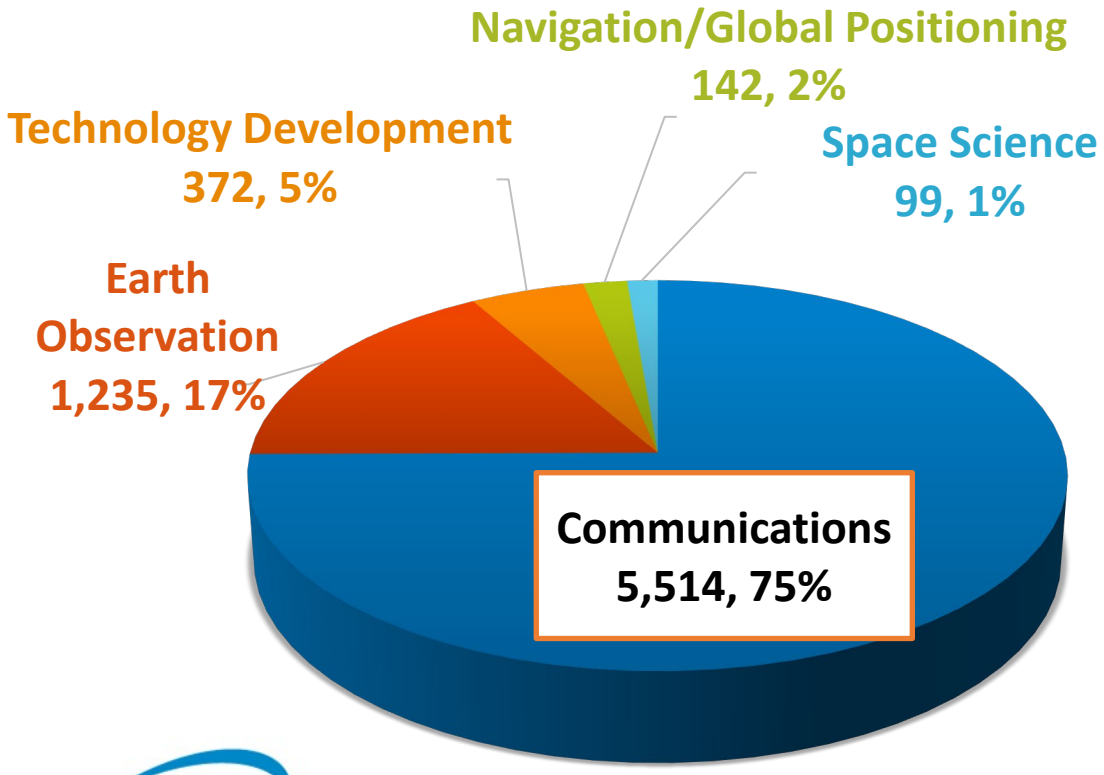
the Future of Memory and Storage

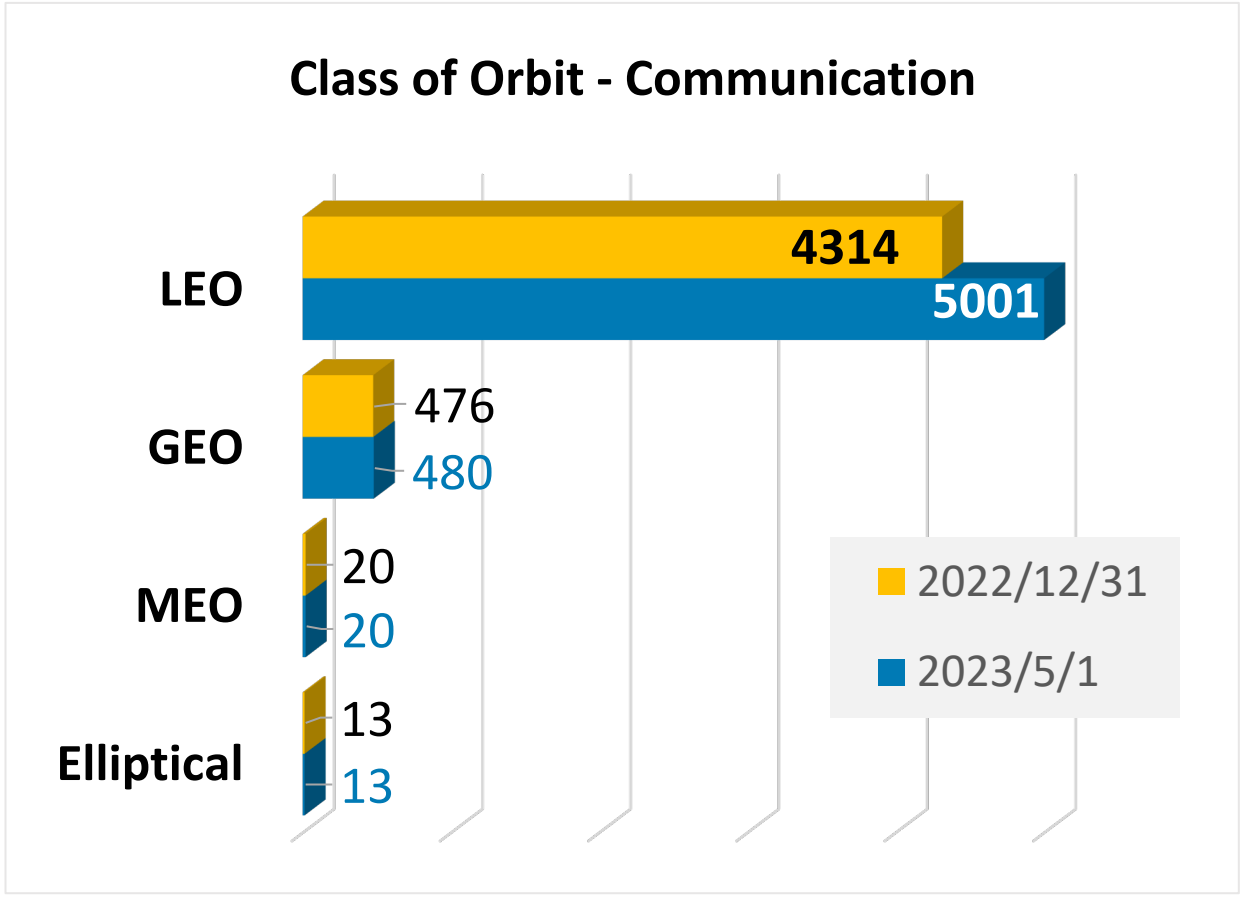
Agenda

- Satellites Quick Facts
- TID test condition and simulation by altitude
- ECC Analysis after TID (40krad) Test
- Environment Measured Single Event Upsets
- End-to-end Data Path Protection
- Conclusion

Satellite Quick Facts

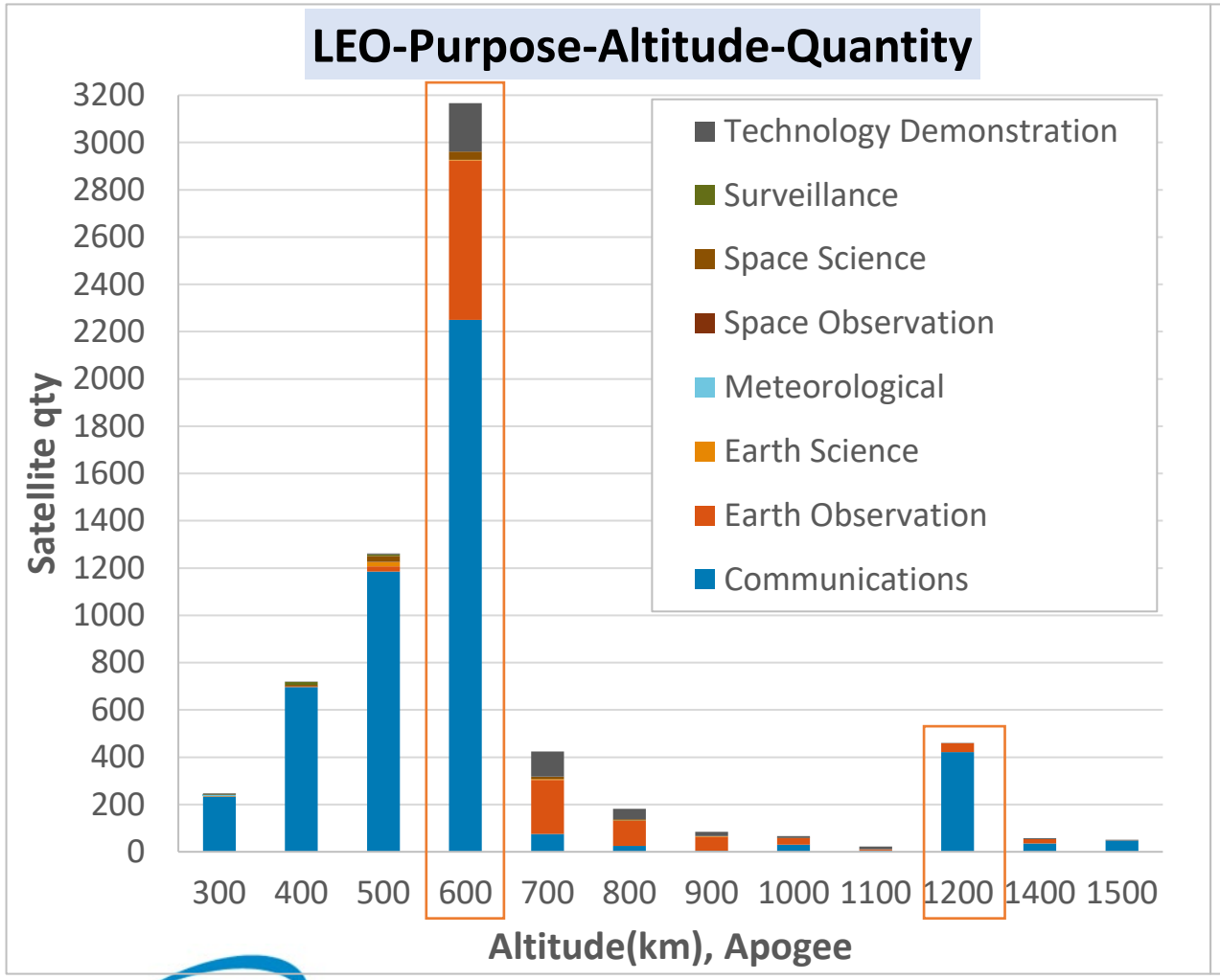
Total number of operating satellites:7,560

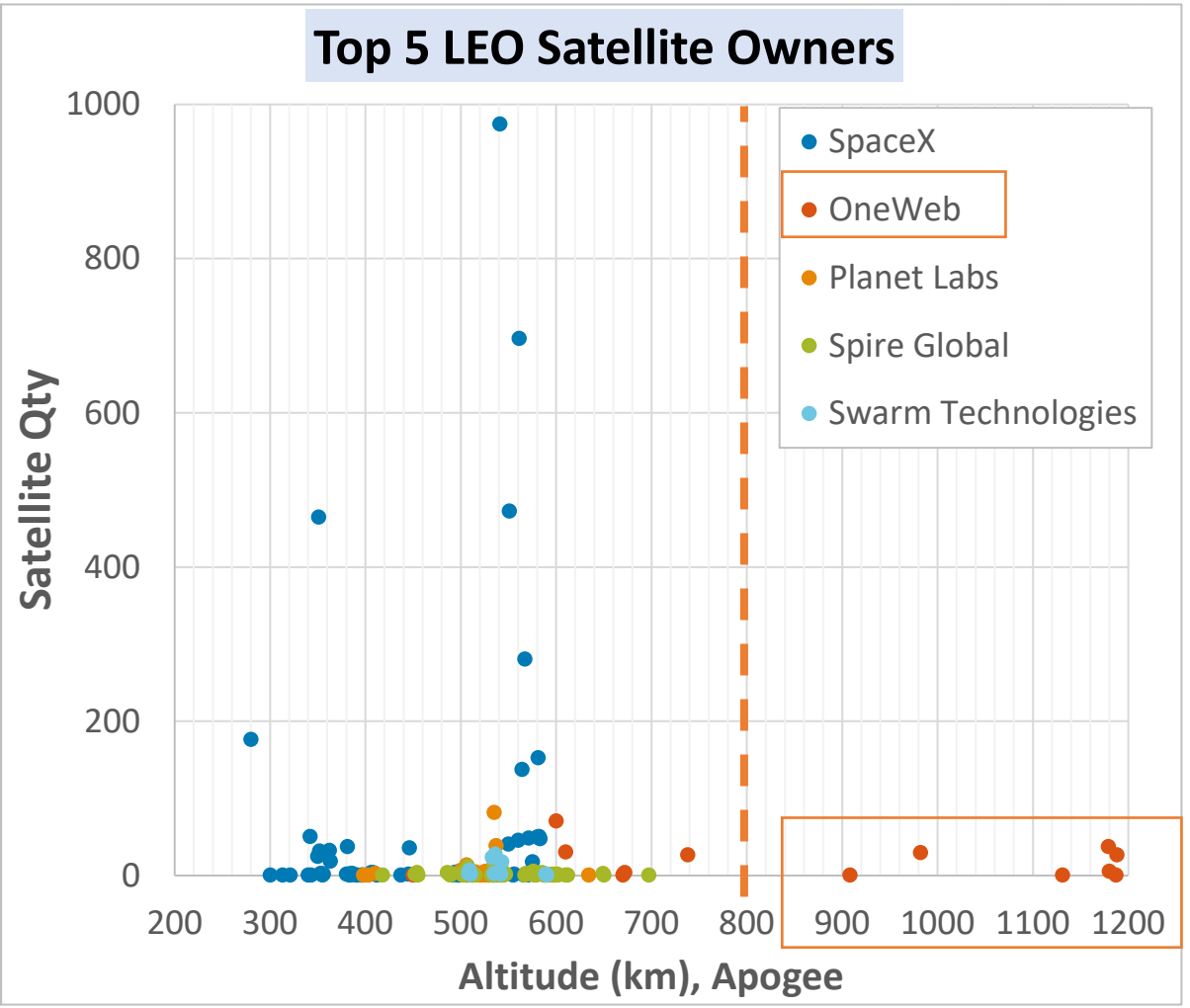




Data source: UCS Satellite Database, as of 2023/05/01

Altitude (km) distribution of LEO Satellites





Data source: UCS Satellite Database, as of 2023/05/01

Space Irradiation Tests

TID (Total Ionizing Dose) irradiation test

- **Cumulative (dose) effects** result from **long-term exposure** to a radiation environment, mostly due to electrons and protons.
- Typical Unit: Gray (Gy) or **KRad (Si)** * 1Gy = 100rad

SEE (Single Event Effects) irradiation test

- SEE caused by **single Ionizing particle strike**/interaction
- Use **protons** or **heavy Ions** to simulate the radiation environment
- Proton SEE irradiation test
- Heavy Ion SEE irradiation test
- Typical Unit: LET (linear energy transfer) **MeV (mg/cm^2)**

Irradiation Test Conditions (TID)

- **Test Conditions vary depending on Mission requirements**
  - With America recently reducing its end-of-life de-orbit requirements from 25 to 5 years (and other nations expected to follow suit), it has limited the altitude range for lower-cost craft.
  - TID for COTS (commercial-off-the-shelf) could be in a range of 7krad(Si), which may be sufficient for lower LEO applications (<600km) with suitable aluminum shielding.
  - However, most 5-year LEO missions require 30krad~50krad(Si) and the DUT (e.g. SSD) is without shielding during the irradiation test.
  - The following TID simulation examples are based on 5mm aluminum shielding (lower number of TID, which fits in the real application)

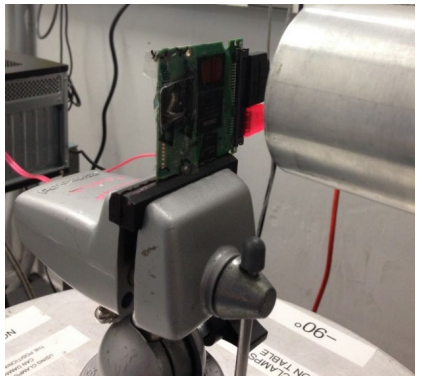


Photo Credit:

Dakai Chen, code 561, NASA Goddard Space Flight Center, Greenbelt, MD 20771 Carl Szabo and Alyson Topper, ASRC Space and Defense, c. o. NASA Goddard Space Flight Center, Greenbelt, MD 20771

At Texas A&M University Cyclotron facility

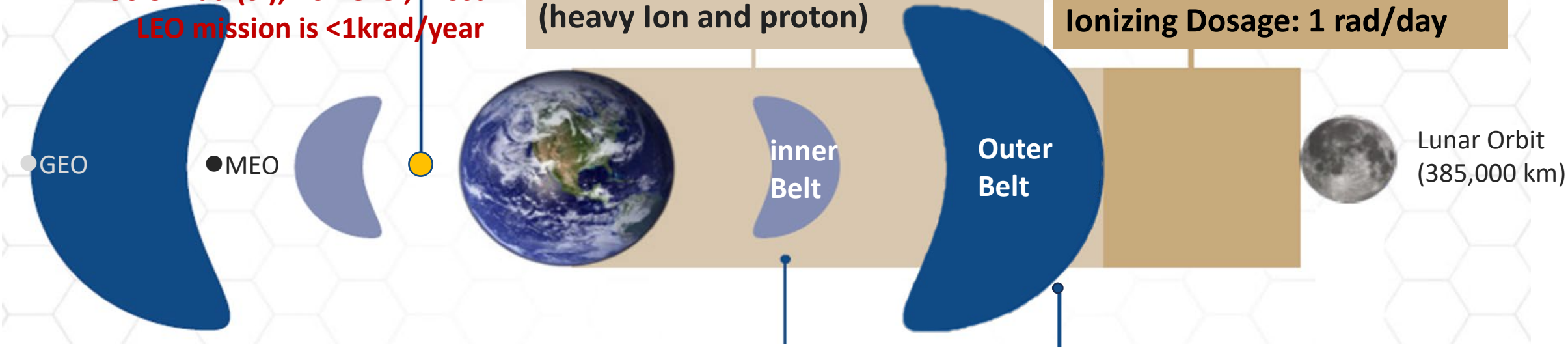
Radiation Environment **Van Allen Radiation Belt**

Low-Earth Orbit <2,000 km

TID: 20rad x 365 days x 5 years
= 36.5 krad (Si), however, most LEO mission is <1krad/year

Near-Earth Env.
Radiation trapped by the earth's magnetic field: max. 20 rad/day (heavy Ion and proton)

Interplanetary Env.
Outside the shielding effects of earth's magnetic field
Ionizing Dosage: 1 rad/day



Inner Belt (1,000 – 12,000 km)
Electrons ~ hundreds of keV
Protons exceeding 100 MeV

Outer Belt (20,000~40,000 km)
High Energy Electrons:
0.1 – 10MeV

Source: Astrobotic 2021/8, wikipedia

TID Level in LEO application (1)

by altitude

- Based on the simulation model

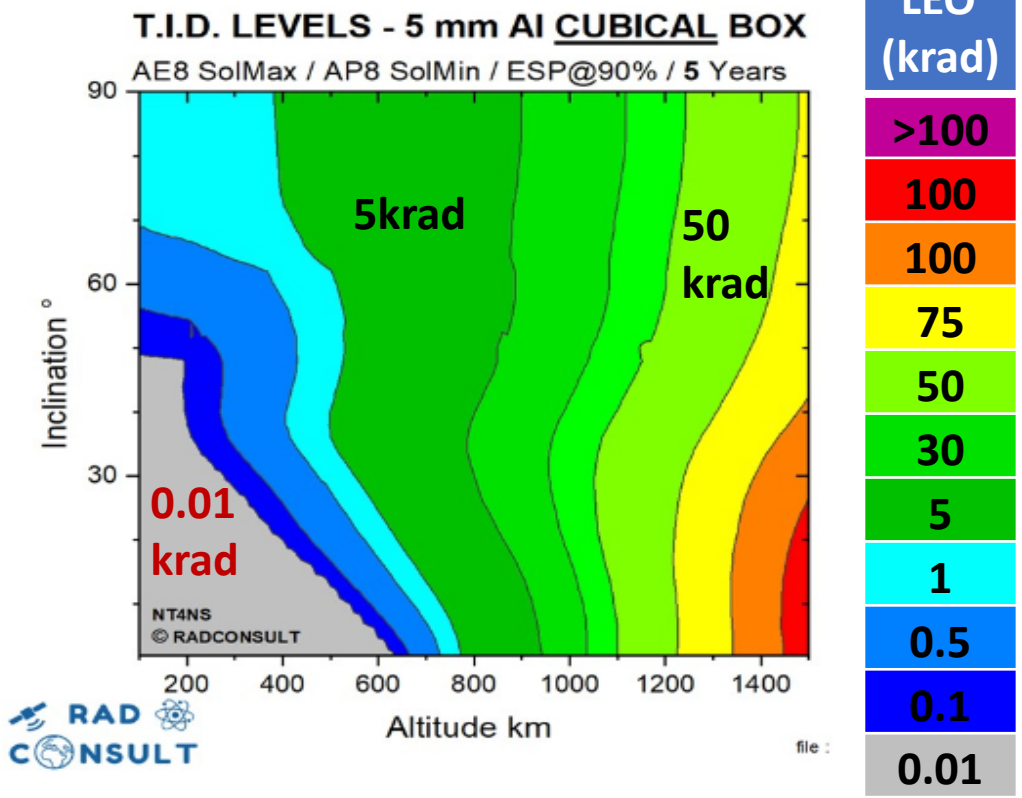
  TID4NS (Total Ionizing Dose 4 New Space)

- 5-year mission
- With 5mm aluminum shielding
- TID:50krad (~1200km)
- TID:5krad (~800km)
- TID:0.01krad (~600km) *could be underestimate

Source: Rad Consult, 2021

***Data for reference only**

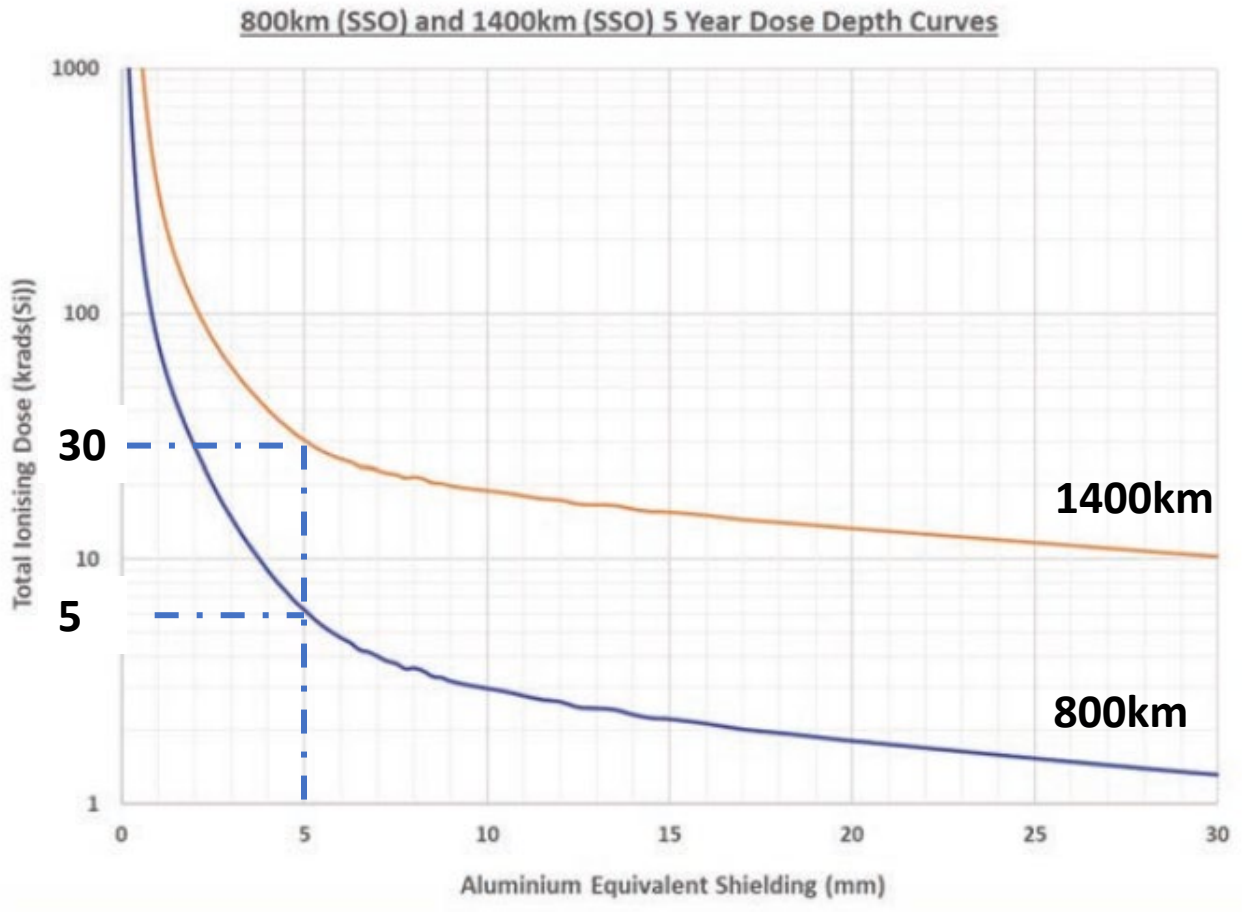
5mm Aluminum Shielding



LEO (krad)
>100
100
100
75
50
30
5
1
0.5
0.1
0.01

TID Level in LEO application (2)
by shielding (mm)

- Based on the simulation model OMERE software by Trad
- 5-year mission
- With 5mm aluminum shielding
- TID:30krad (1400km)
- TID:5krad (800km)



Source: Source: COTS The Inevitable March to the Van Allen Belt, https://doi.org/10.59332/jbis-076-11-0371

TID Level in LEO application (3)
by altitude, trapped protons

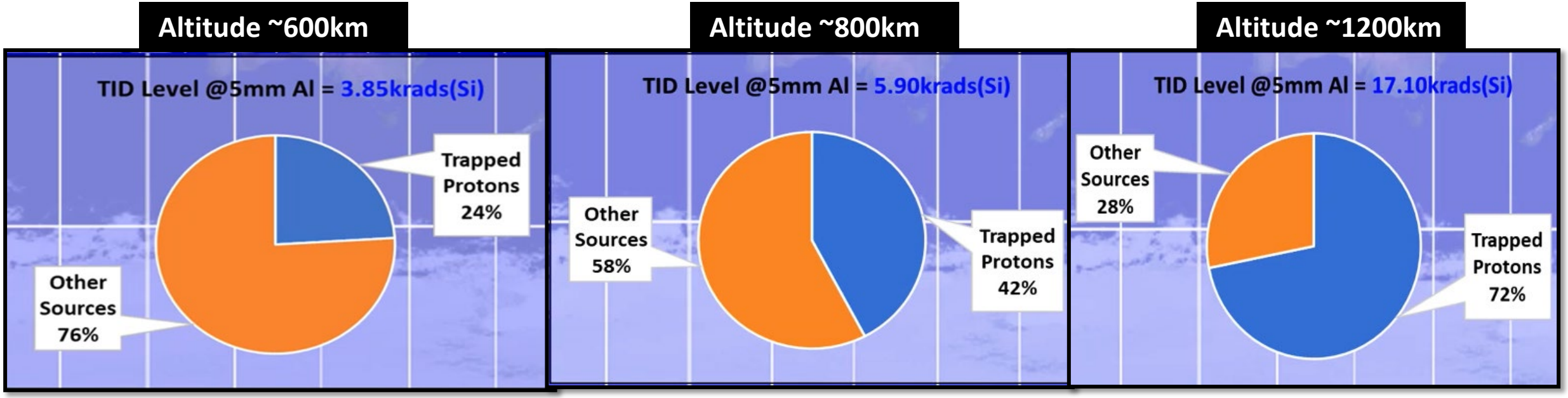


Photo Source: RASL

- Based on the simulation model OMERE software by Trad
- 5-year mission, With 5mm aluminum shielding
- **In higher LEO orbits 1000 km+), increasing trapped protons**

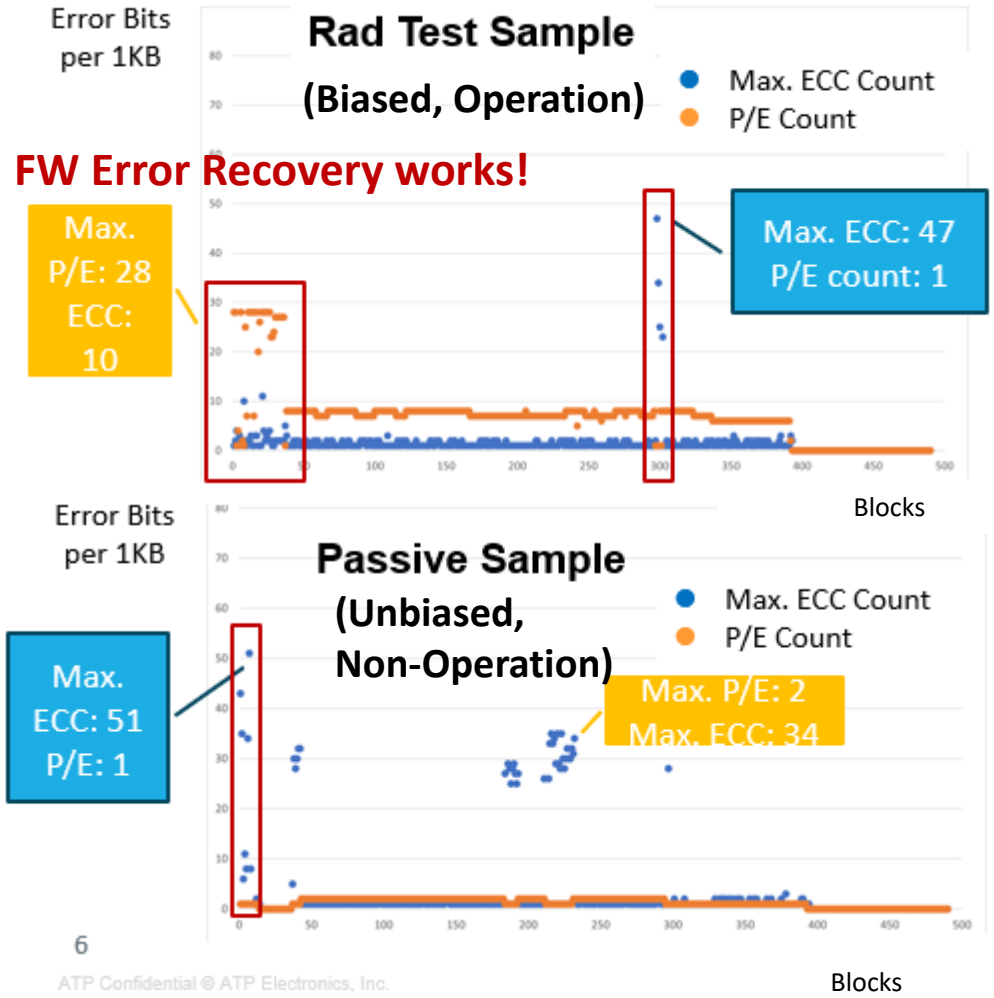
ECC Analysis after TID (40krad) Test

- With a gamma radiation source (Co-60)
  - Rad Test Sample (operational during TID test)
  - Passive sample as a cold spare (not mounted)
  - **Before the TID test, 100% NAND ECC screening is conducted on both samples.**
  - **Micron 64L 3D TLC (SLC mode)**
  - The biased and operational one was used with OBC and performed well until the end of the test – 40krad(Si) which corresponds to a 10-year-long mission in LEO.

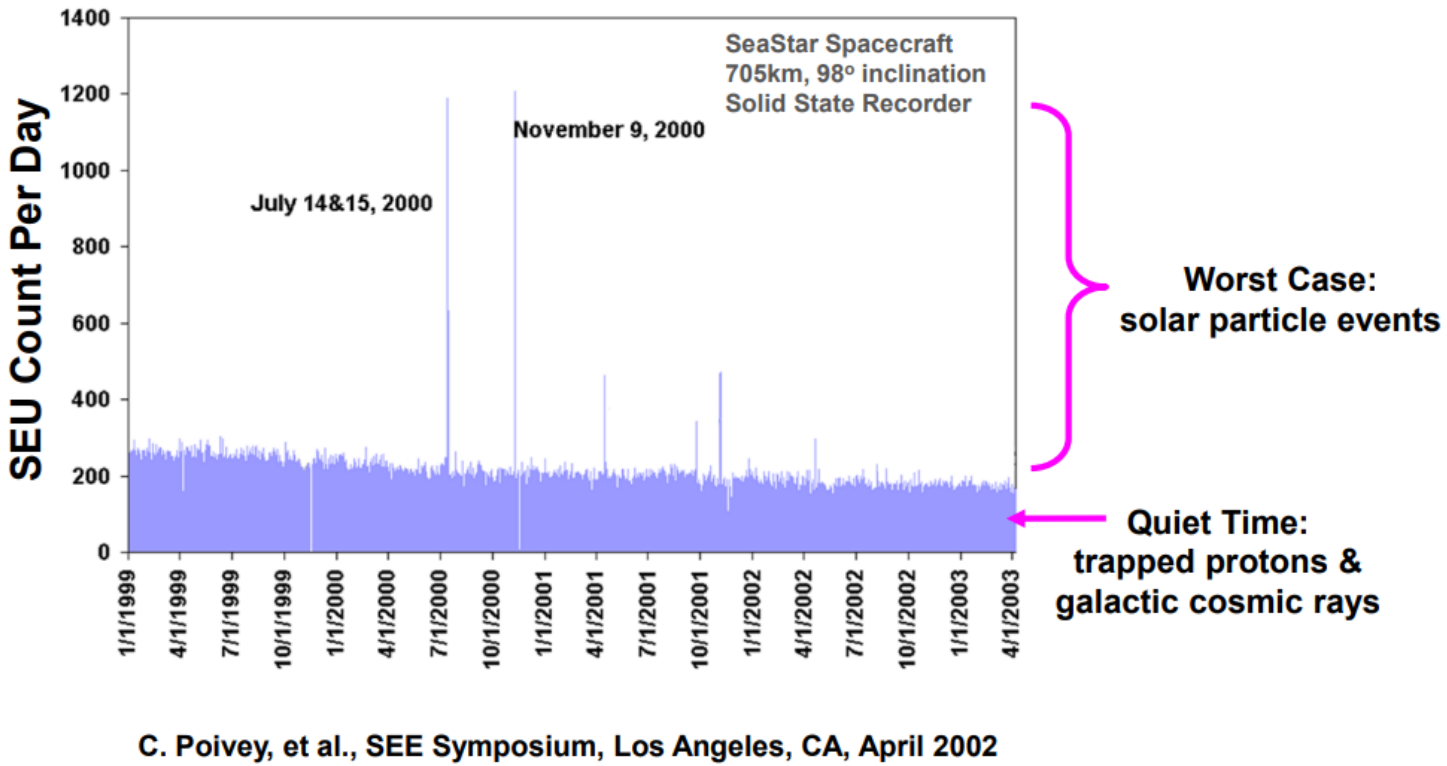
Findings:

- **No later bad blocks (No UECC) in both samples.**
- **Unbiased/non-operation sample: higher error bits than the Biased/operation sample.**
- **More Operations, Lower Error rate!**

During operations, the FW error handling mechanism helps to recover errors.



Example Environment Measured Single Event Upsets



C. Poivey, et al., SEE Symposium, Los Angeles, CA, April 2002

- In higher LEO orbits 1000 km+, a higher % of the mission is within the inner Van Allen Belt, with much higher SEE risk due to **trapped protons & GCR (Galactic Cosmic Rays)**
- Shielding can reduce rates during solar events.
- However, GCR rate with a lower limit for SEU, which is not practical to reduce.
- SEFI (Single-Event-Functional-Interrupt) can be recovered by power cycling in most cases.

Reduce Soft errors and Data Integrity

Controller SRAM	DRAM	NAND Flash
• SECDED* • E2E**: 32 bits data with 8 bits parity • HW IP, can be verified by error injection	• SECDED* • E2E**: 32 bytes data with 2 bytes parity • HW IP, can be verified by error injection	N/A
• SRAM **doesn't need to be refreshed** as its circuit design does not result in a charge drain.	• **More Refresh Cycles** (frequency, temp.)	• **RAID Parity** • **LDPC** • **Read Retry**
ULA (Ultra-Low-Alpha) Package		

*SECDED: Single Error-bit Correction, Double Error-bit Detection
**E2E: End-to-End Protection

SSD End-to-End Data Path Protection

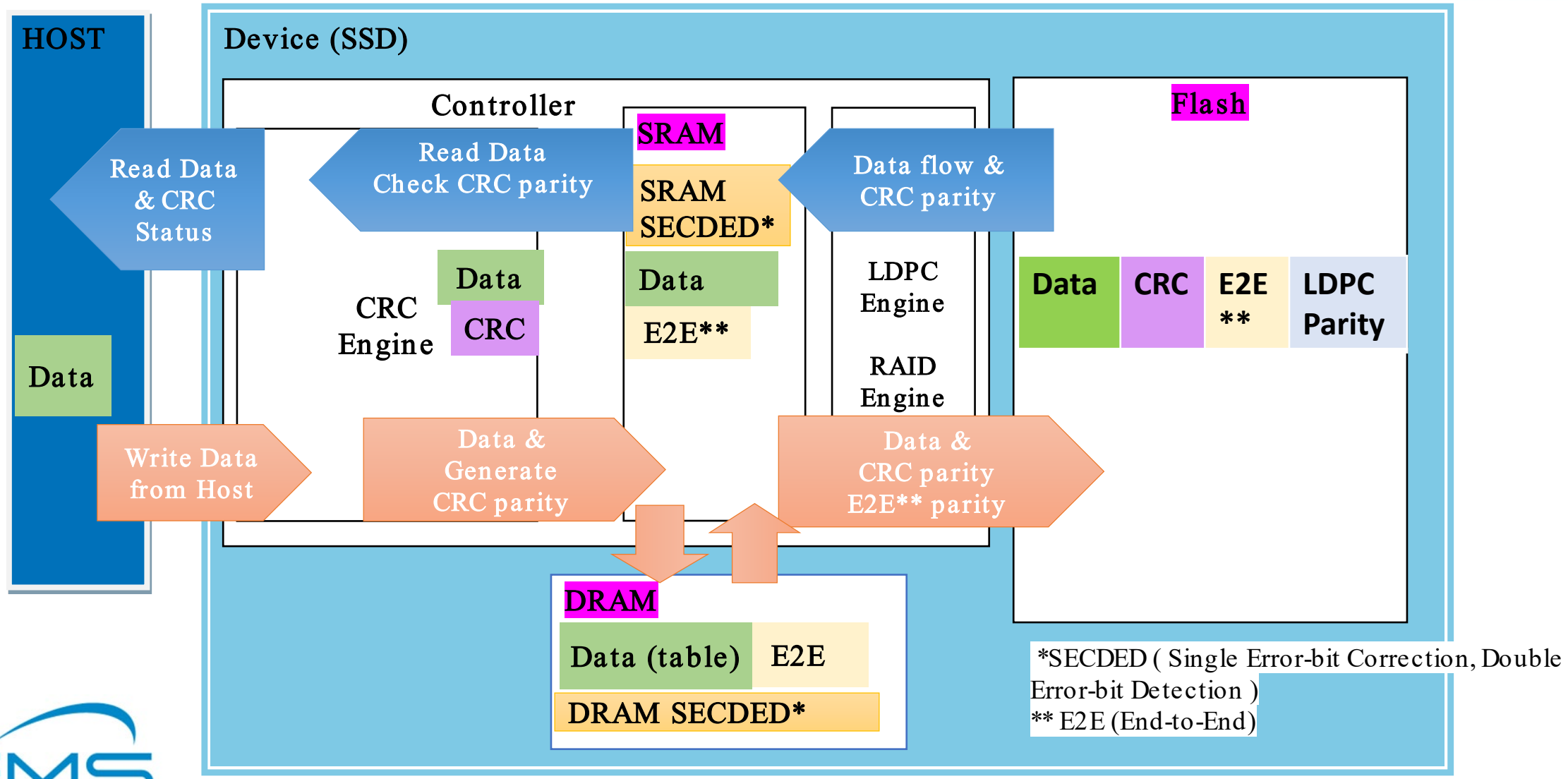
Buffering Data: DRAM (optional) & SRAM (controller)

- Soft errors
- **SECDED** (Single Error-bit Correction, Double Error-bit Detection)
- E2E (End-to-End) protection, generate E2E parity
- More refresh cycles (DRAM)

Storage Data: NAND Flash

- **RAID Parity:** calculating a parity bit (or block) for a set of data blocks. This parity bit is used to detect and correct errors. The calculation typically uses an XOR (exclusive OR) operation, which ensures that the parity bit can help reconstruct data if one of the disks fails.
- **LDPC** (**L**ow-**D**ensity-**P**arity-**C**heck) Engine & **Read Retry**

SSD End-to-End Data Path Protection - Block Diagram



DRAM Refresh Cycles & Refresh Periods

- JEDEC Standard No. 79-4D
- More refresh cycles or shorter refresh periods at high temp (similar concept can be applied to reduce soft errors)

  Example of Micron DDR4

Features

- T_C = 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

- Some systems also "scrub" the memory, by periodically reading all addresses and writing back corrected versions if necessary to remove soft errors.

Table 43 — tREFI and tRFC parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)		7.8	7.8	7.8	7.8	us
1X mode	tREFI1	0°C <= TCASE <= 85°C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	us
		85°C < TCASE <= 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
	tRFC1(min)		160	260	350	550(default) 450 (optional-1) 350 (optional-2)	ns
2X mode	tREFI2	0°C <= TCASE <= 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
		85°C < TCASE <= 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
	tRFC2(min)		110	160	260	350(default) 350 (optional-1) 260 (optional-2)	ns
4X mode	tREFI4	0°C <= TCASE <= 85°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
		85°C < TCASE <= 95°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	us
	tRFC4(min)		90	110	160	260(default) 260 (optional-1) 160 (optional-2)	ns

Note 1 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. tRFC2 and tRFC4 needs to be set corresponding to each setting's value (default / optional-1 / optional-2) accordingly. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

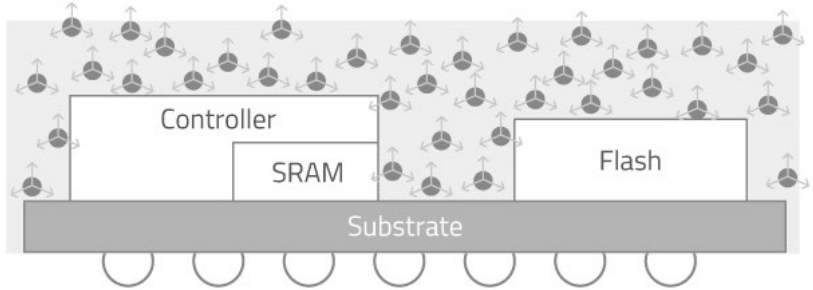
4.9.3 Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 18, when REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

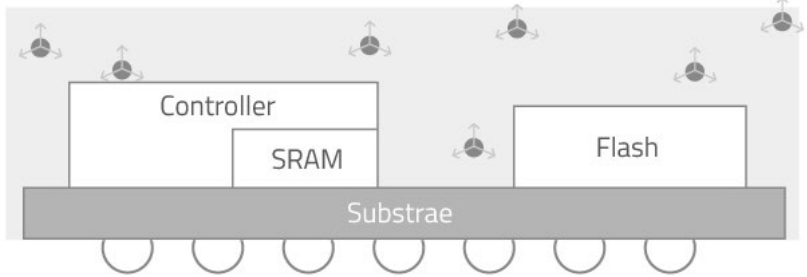
Ultra Low Alpha Particles Packaging Materials

As demand for higher density (thinner silicon), functionality (denser circuitry), and lower power, the electronic devices' sensitivity to radiation increases dramatically.

Normal Mold Compound



Ultra Low Alpha (ULA) Mold Compound

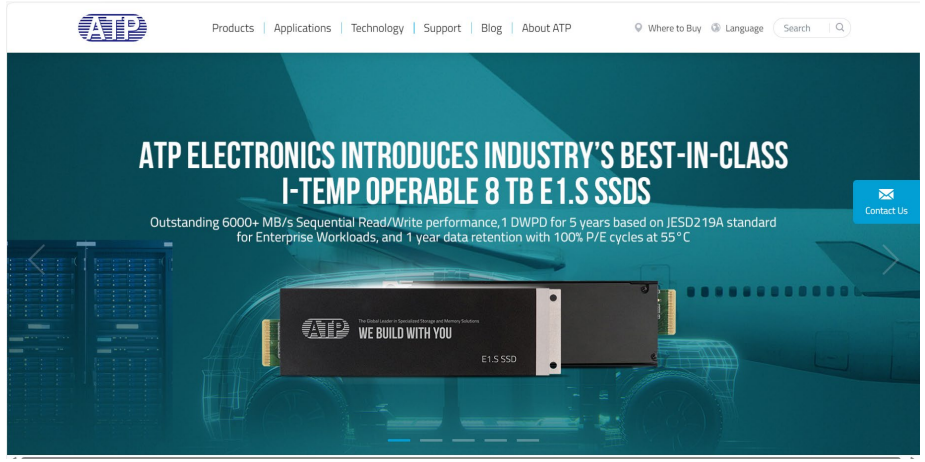


Conclusion

1. **Large opportunities for higher density SSD in LEO applications, esp. Satellite communication and Remote Sensing**
2. **Choose Product/component wisely**
   - **Understand Mission Requirements (mission life, altitude) considering TCO (total cost of ownership) no overkill or underestimate.**
   - **Choose ECC Memory: SECDED** (Single Error-bit Correction, Double Error-bit Detection) helps to recover memory soft errors
   - **Powerful Controller FW algorithm helps to reduce/recover errors**
3. **Additional Efforts help to reduce errors**
   - **More refresh cycles as needed on DRAM**
   - **Ultra-Low-Alpha packaging materials**
   - **100% NAND Screening in Mass production of each product**

For More Information on ATP Electronics

Visit our website: www.atpinc.com



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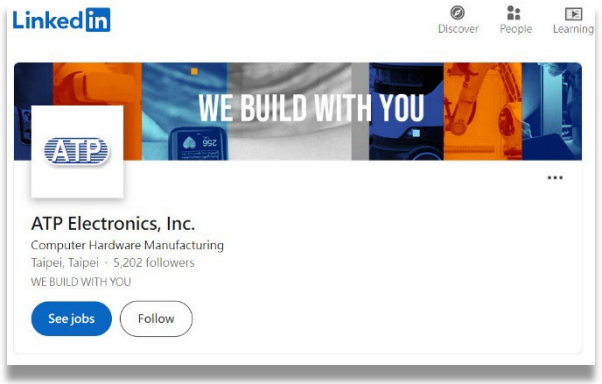

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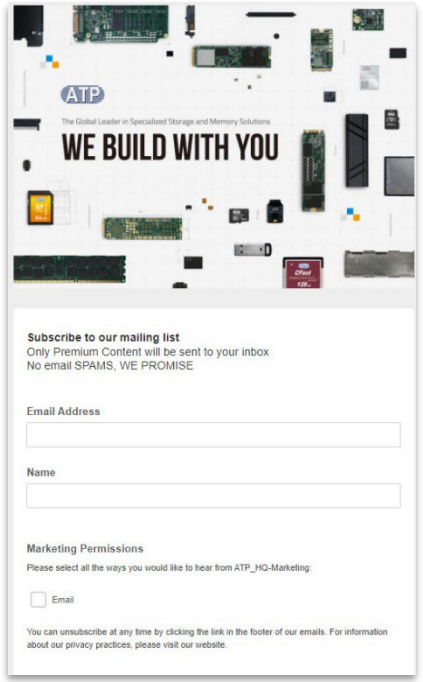

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Thank you!