

BBCube 3D: Heterogeneous 3D Integration Using WoW/CoW for Near Memory Computing

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the Future of Memory and Storage



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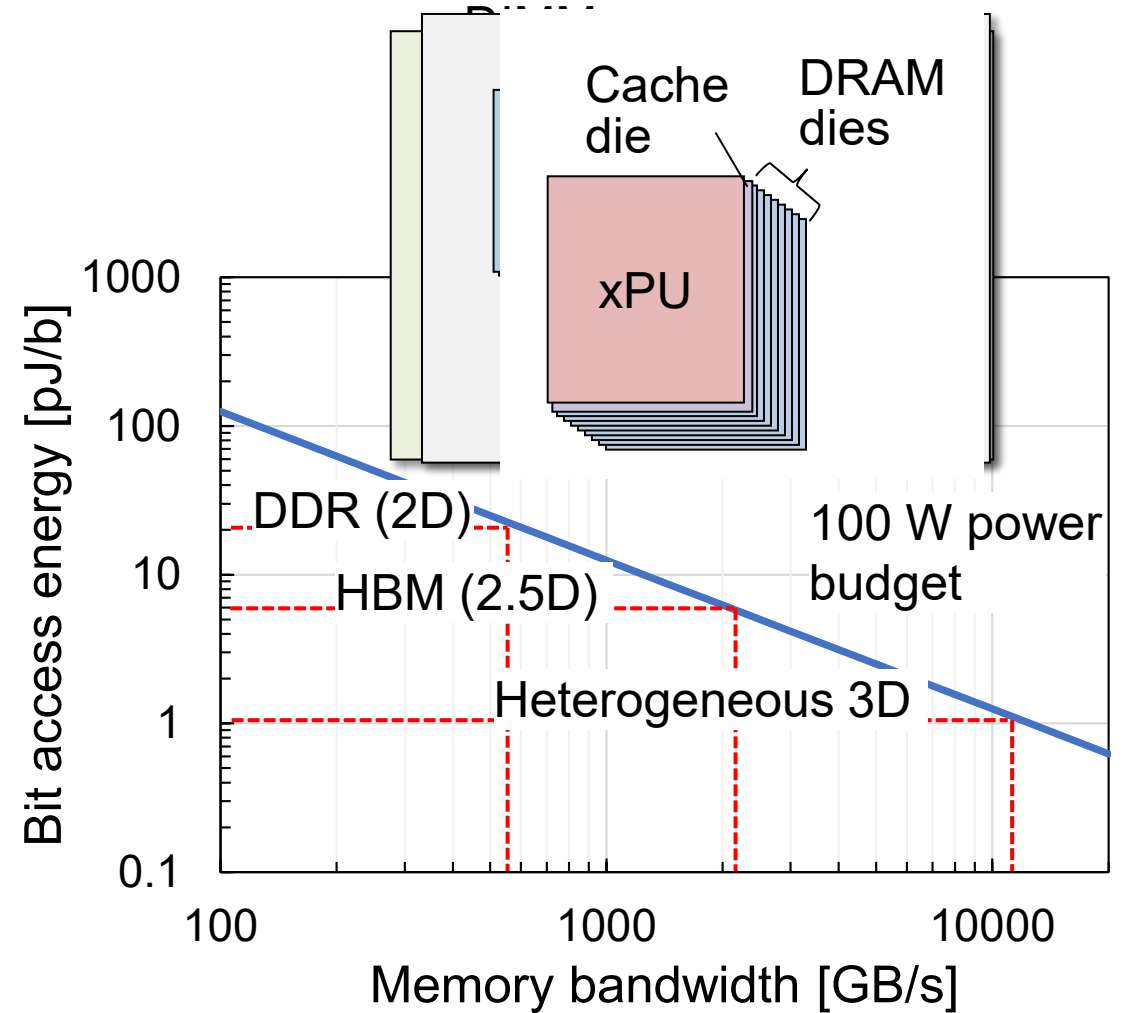
Outline

- Motivation
- Analysis Models
- Analysis Results (Thermal)
- Analysis Results (Electrical)
- Conclusion



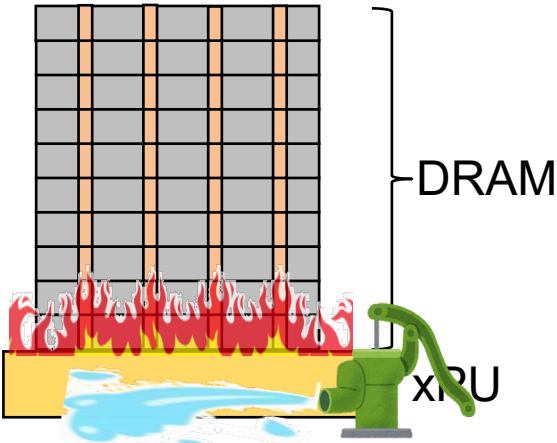
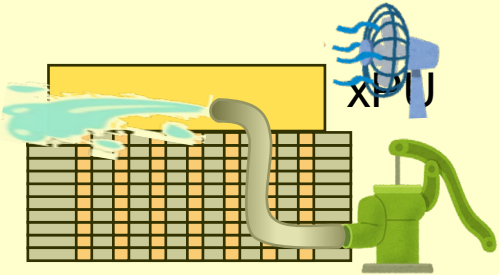
Motivation

- Demands for high data bandwidth are increasing
- HBM has been introduced
 - High bandwidth with the same power
 - 2D transmission prevents improvement of access energy
- Heterogeneous 3D integration
 - Paving the way to 10 TB/s



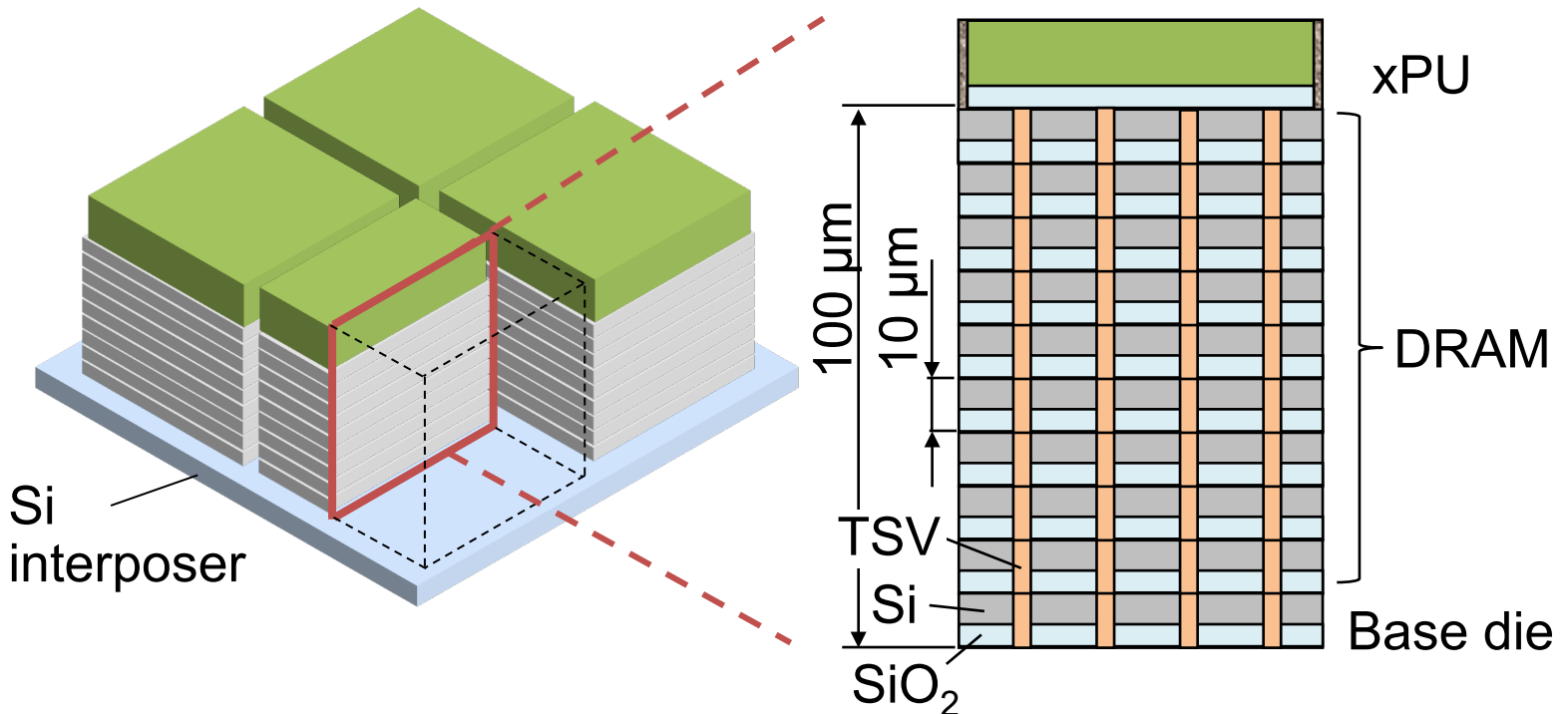
Heterogeneous 3DI challenges

- Cooling
 - xPU cannot dissipate heat sufficiently
- Power delivery
 - Impedance of TSV causes supply voltage drop and large droop
- BBCube has potential to solve 3DI issues
 - Dense TSVs
 - Thin dies

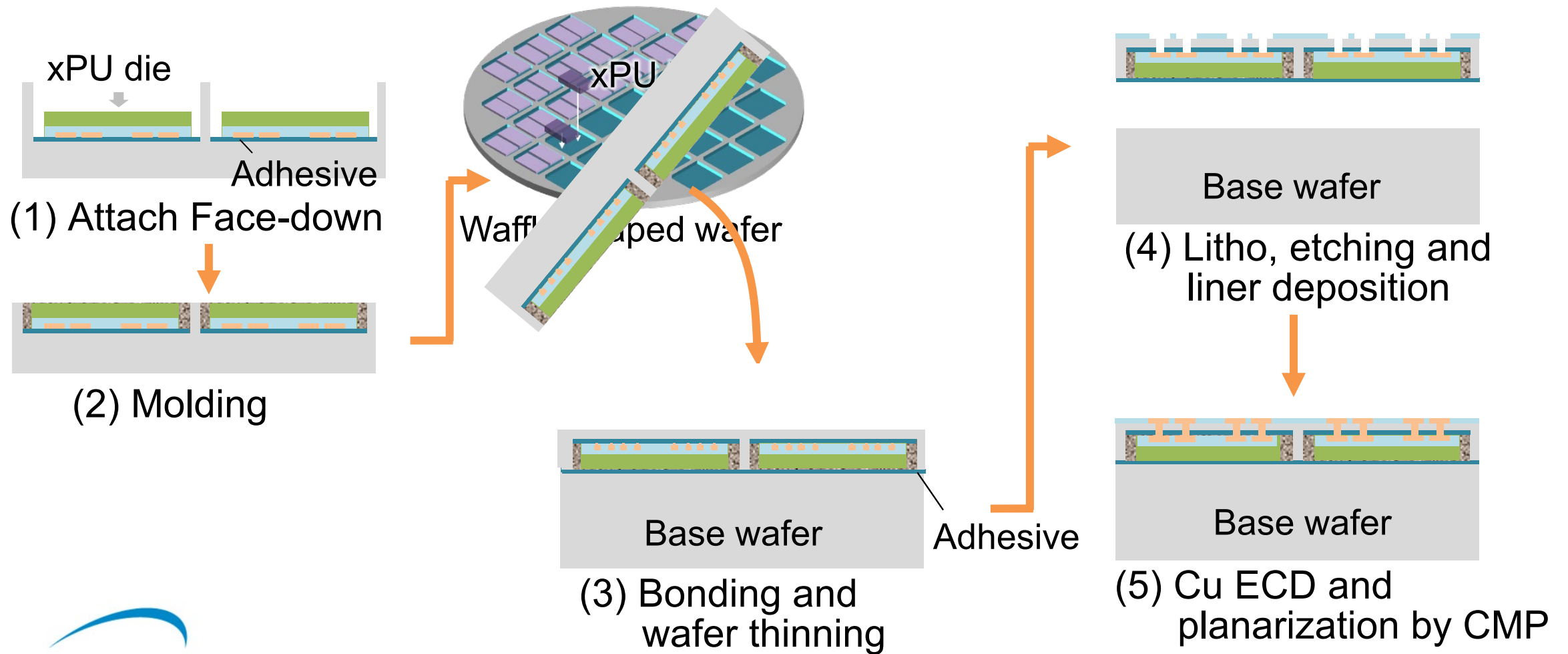
	Memories on top of xPU	BBCube 3D
Structure		
Cooling	Difficult	Easy
Power Delivery	Easy	Easy

Structure of BBCube 3D

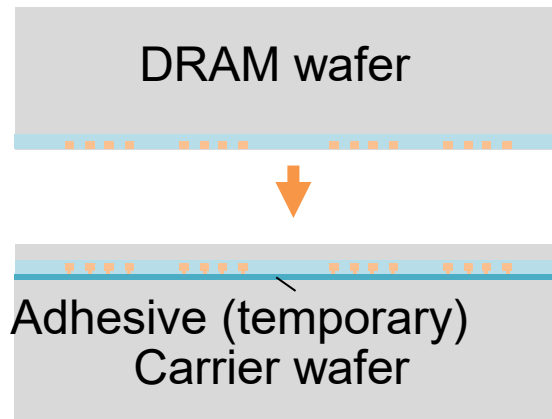
- BBCube 3D comprises
 - Multiple xPU chiplets
 - Last level cache die
 - Laminated DRAMs
 - Base die
- Stacked by WoW and CoW



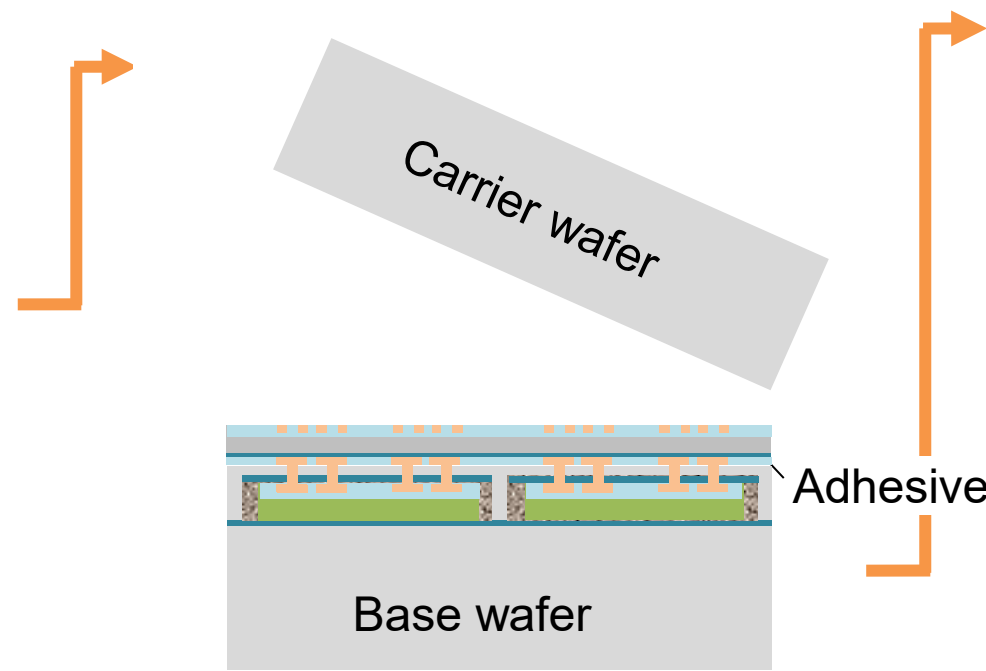
Process Flow of BBCube 3D (CoW)



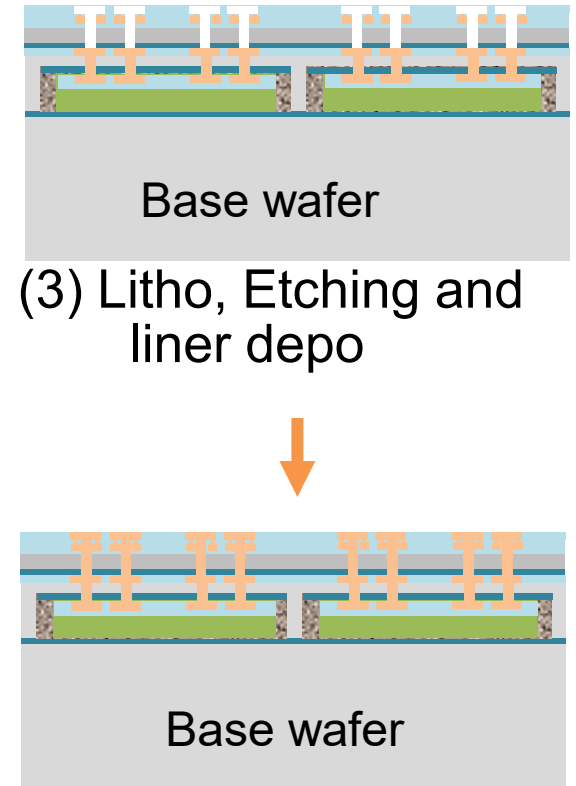
Process Flow of BBCube 3D (WoW)



(2c) Wafer thinning



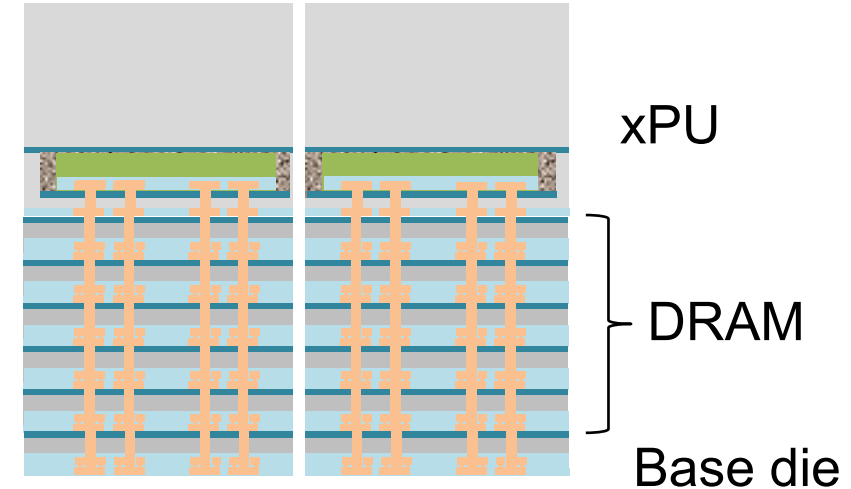
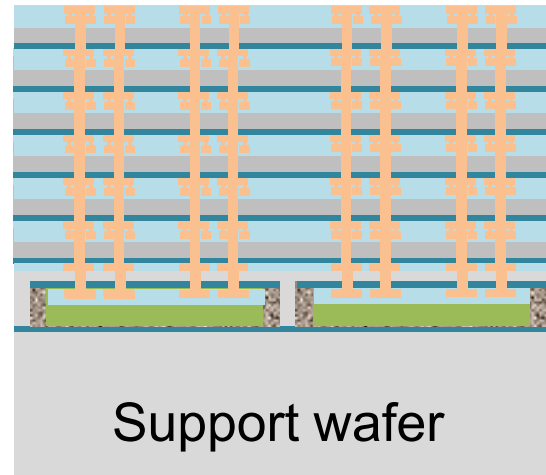
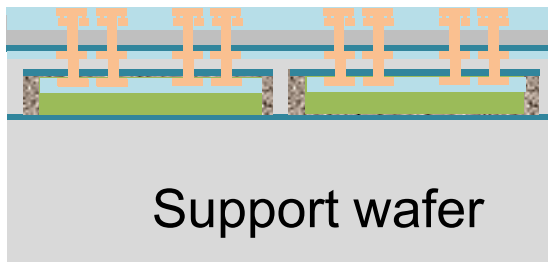
(2) Bonding and debond carrier wafer



(4) Cu ECD and flattened by CMP



Process Flow of BBCube 3D (WoW)

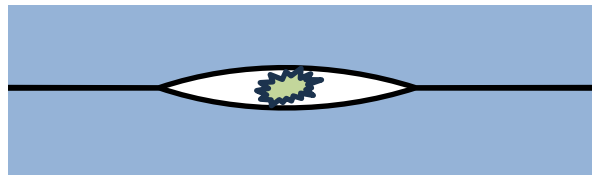


(9) Repeat step 6 to 8

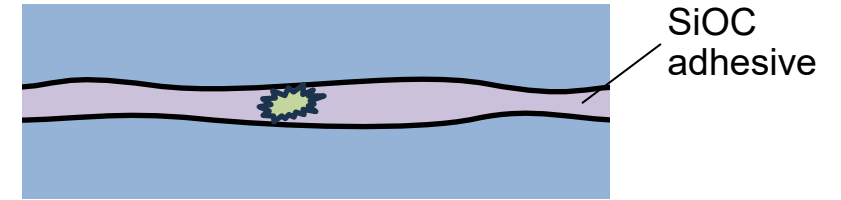
(13) Dicing and singulation

Superior Connectivity of BBCube

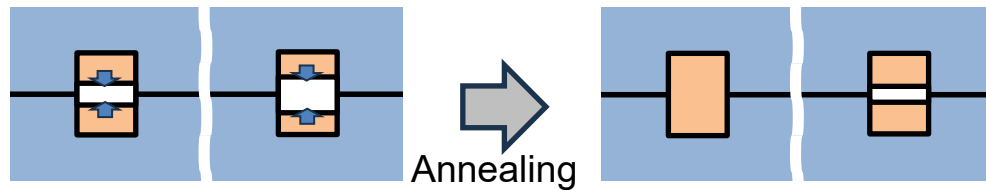
- Bumpless Via-Last interconnect similar to Cu/Low-k BEOL process
 - Stacking and thinning first, TSV formation last
 - Wafer/die bonding used SiOC adhesives. No needs nano-scale planarization
 - BEOL-based high reliability interconnects with low-thermal budget



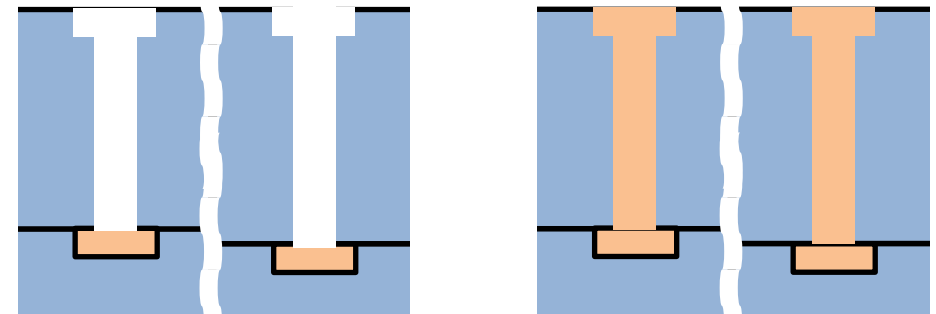
Nanometer-size particles create void



Absorb surface roughness and particles by adhesive layer



Nanometer-level recess control is needed



Etching

Metal deposition



Hybrid Bonding

BBCube

TSV characteristics

- Dense TSV realize high BW
- Short and slim TSV decreases C
- Direct Cu-Cu contact, thin bonding layer decreases R_{th}

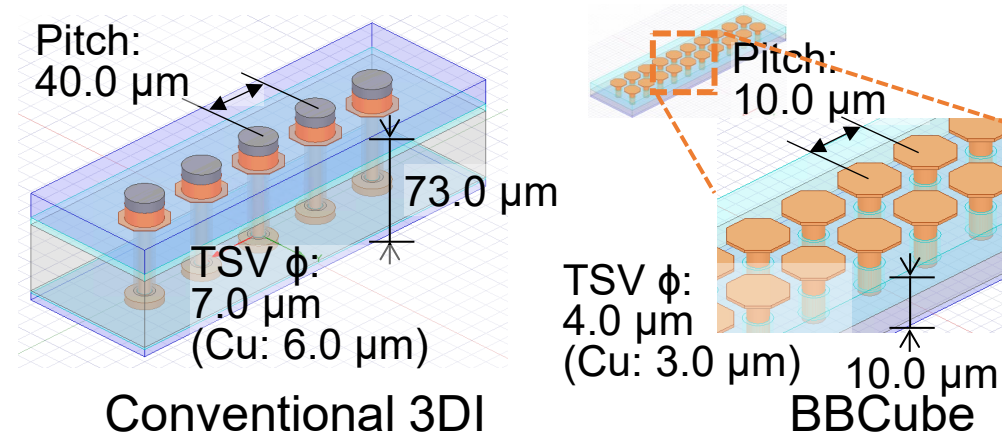


Fig. 1 Physical dimension of TSV

Table 1 Thermal resistance of TSV

	Conventional 3DI	BBCube
Temp. [°C] (Log scale)	<p>Stationary wall: 0 °C</p> <p>Surface heat: 10 MW/m²</p>	<p>Stationary wall: 0 °C</p> <p>Surface heat: 10 MW/m²</p>
R _{th eff} [K mm ² /W]	18.02	0.26

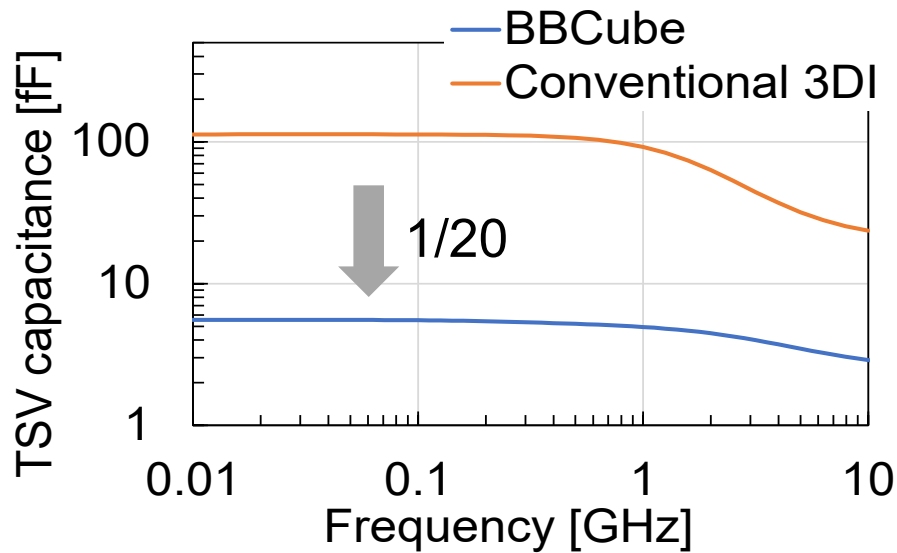
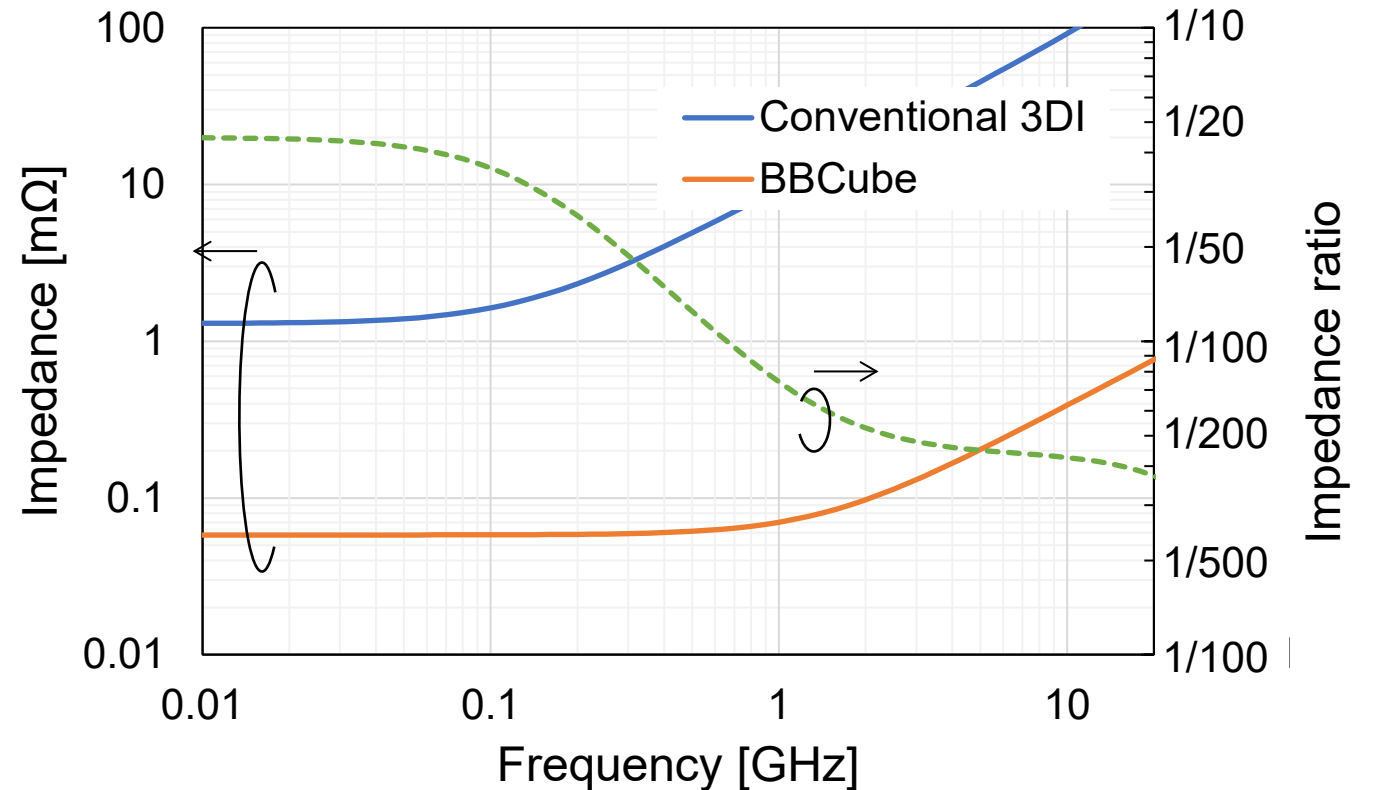


Fig. 2 TSV capacitance

Power supply impedance analysis

- Comparison with BBCube and conventional 3DI in impedance
 - 22-times lower at 10 MHz
 - 220-times lower at 5 GHz
- DC drop is decreased $65.1 \text{ mV} \rightarrow 2.9 \text{ mV}$
 - When 45 W (50 A) xPU is stacked on 8 laminated DRAMs

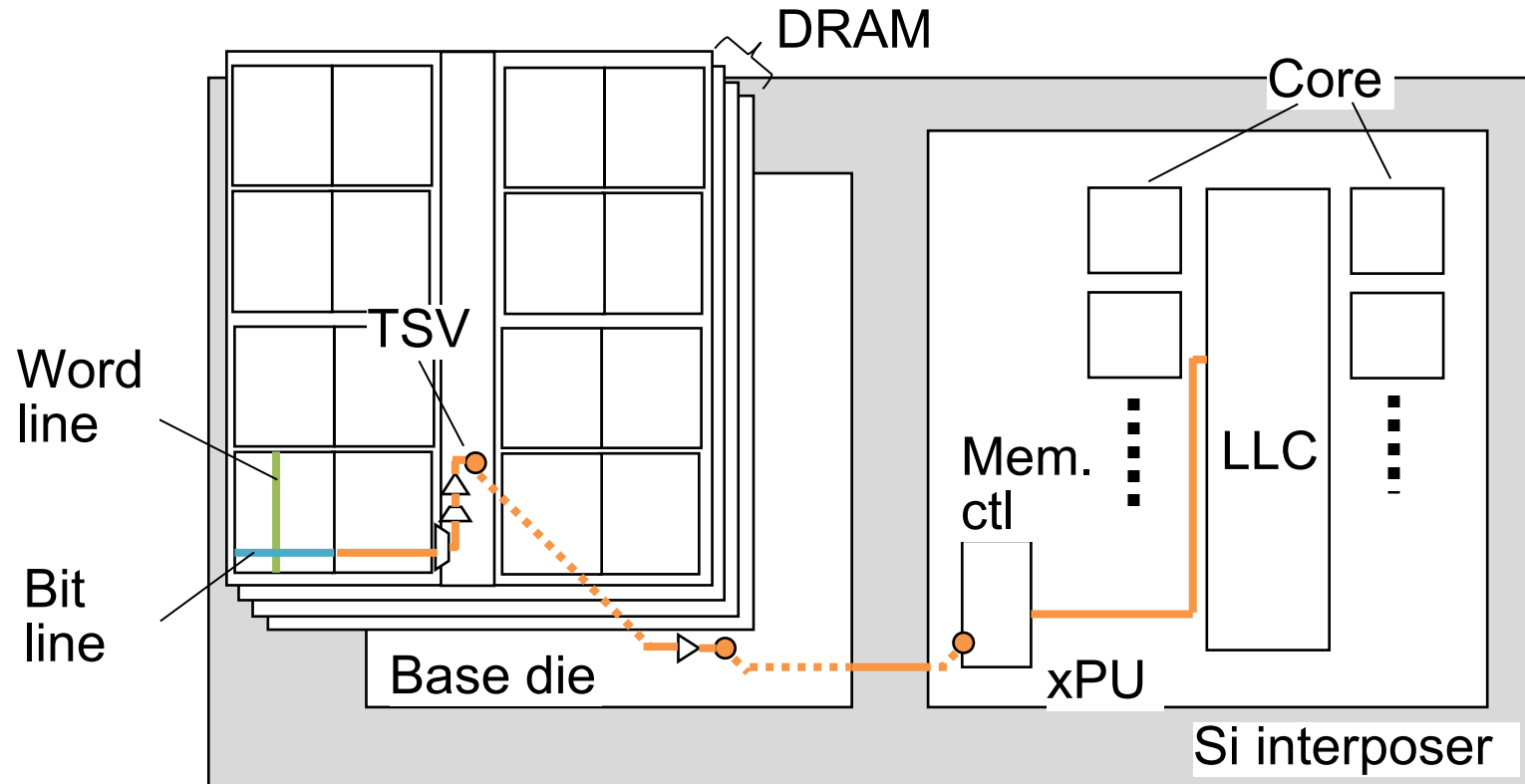


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Bit Access Energy Calculation

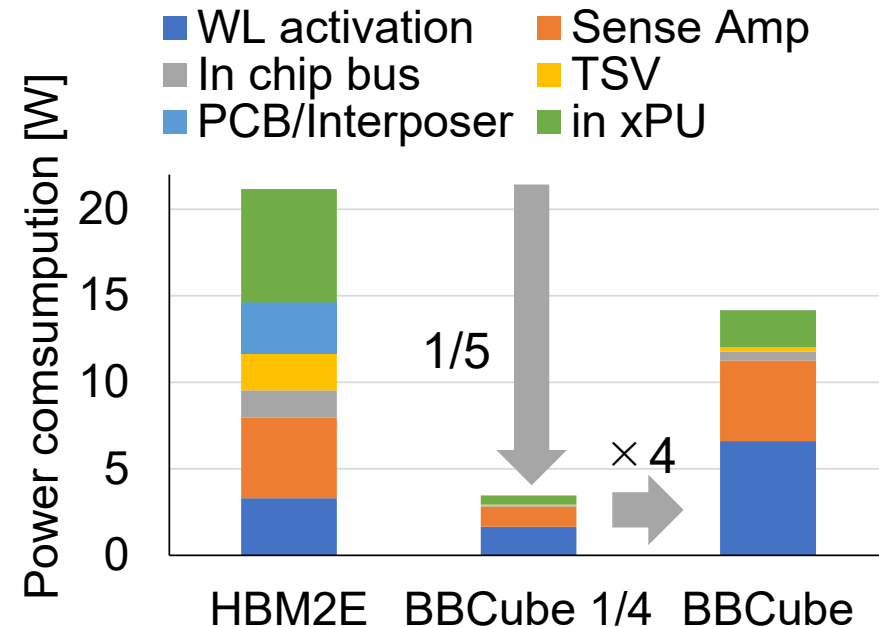
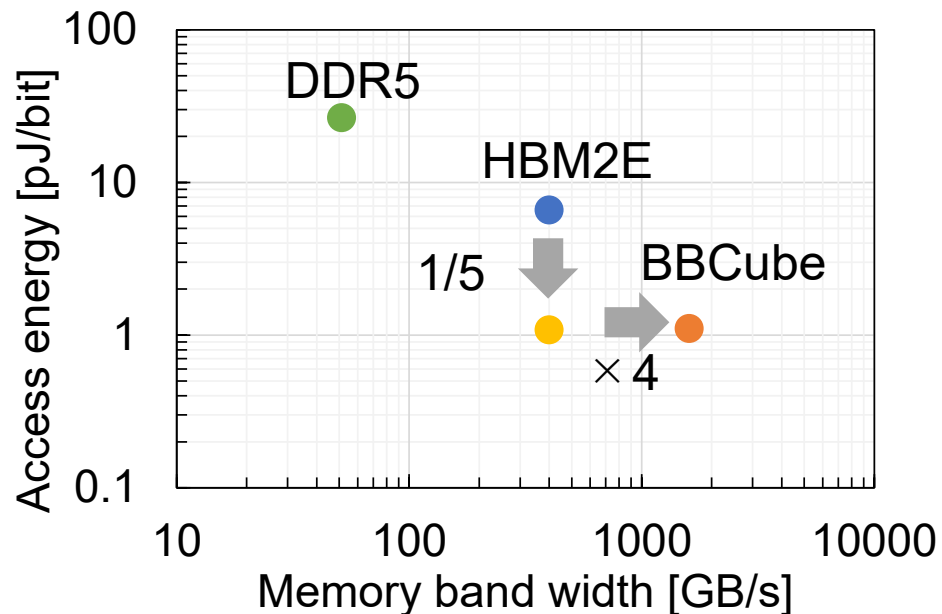
- Calculate energy from row activation to last level cache in xPU



Access route of HBM

Bit access energy

- BBCube 3D reaches
 - 30X higher bandwidth, 20X lower access energy than DDR5
 - 4X higher bandwidth, 5X lower access energy than HBM2E



DRAM temperature

- In BBCube™ 3D, over 47 W xPUs can be stacked
- If $\times 9$ BBCube (\approx reticle size), over 423 W xPUs can be stacked

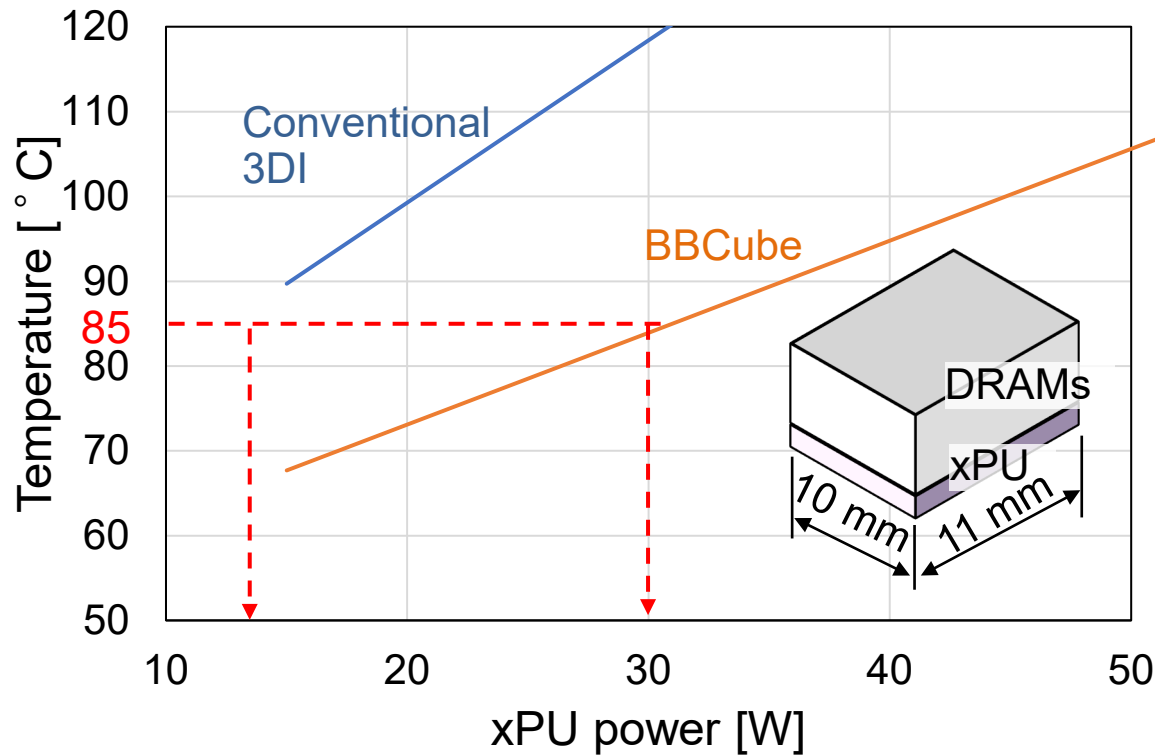


Fig. 1 DRAMs on xPU

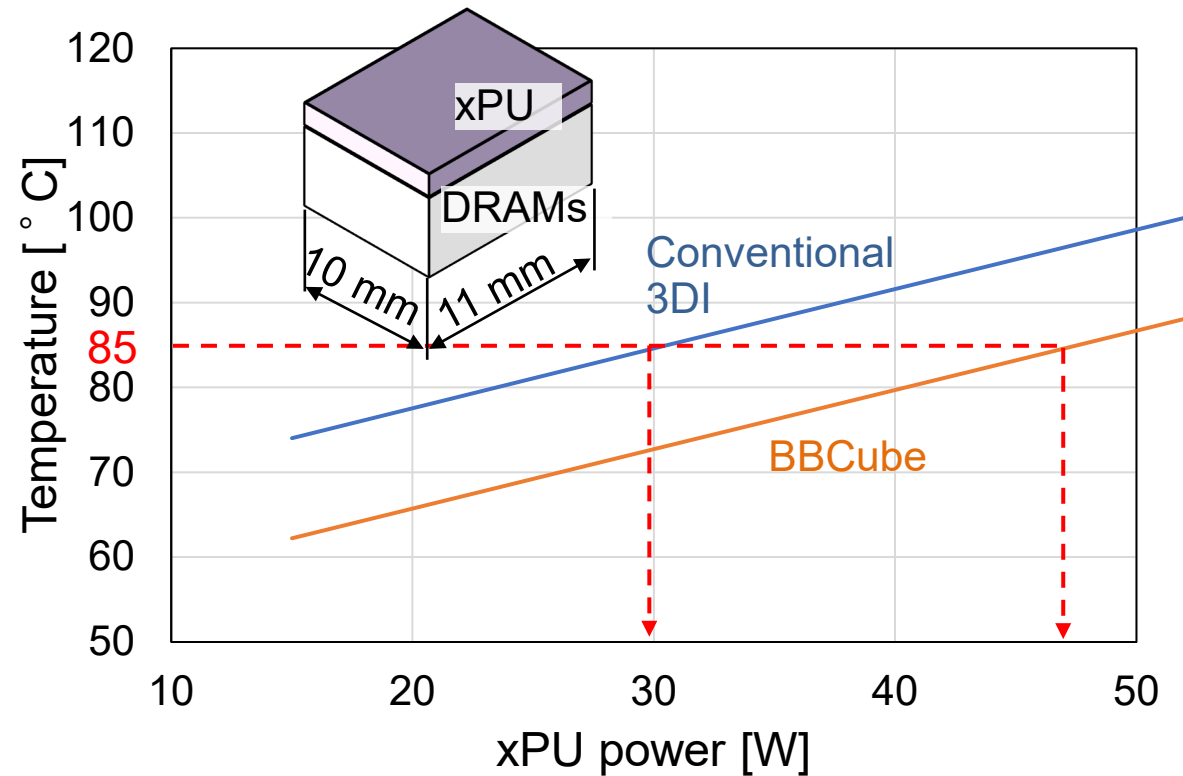


Fig. 2 xPU on DRAMs

Conclusion

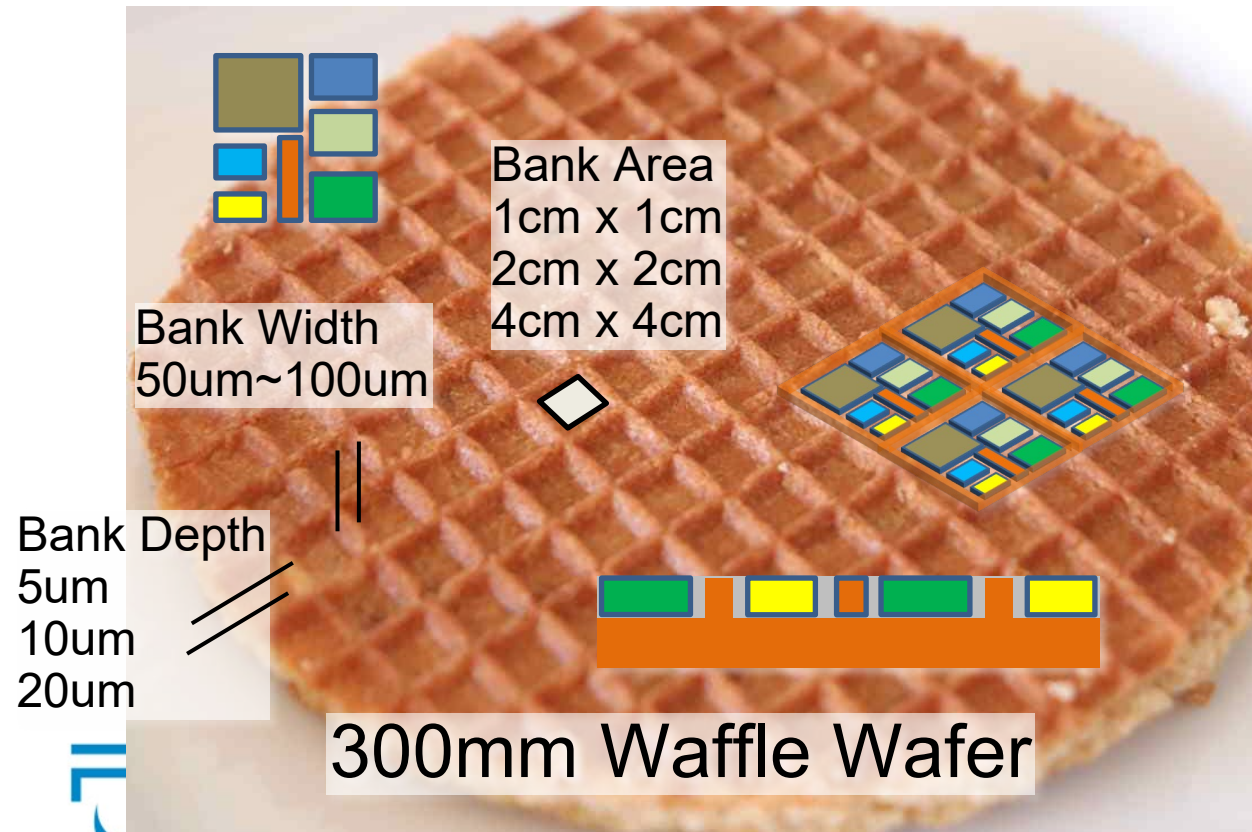
- We proposed a heterogeneous 3DI technology called BBCube 3D
 - Combined use of bumpless WoW and CoW processes with high-density and low-capacitance TSVs
- BBCube 3D achieves
 - High reliability with a low-temp. process
 - 30X higher bandwidth, 20X lower access energy than DDR5. 4X higher bandwidth, 5X lower access energy than HBM2E
 - 45 W xPUs stacked on a DRAM cube. If ×9 BBCube (\approx reticle size), over 423 W xPUs can be stacked



Let's Eat BBCube!

- TECH EXTENSIONS Co. Ltd. (TEX) handles the WoW and CoW stacking by BBCube.

COW Hetero-Stack



WOW/COW Multi-Stack

