CXL Disaggregated Memory Solution for HPC and AI Workloads

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FMS the Future of Memory and Storage

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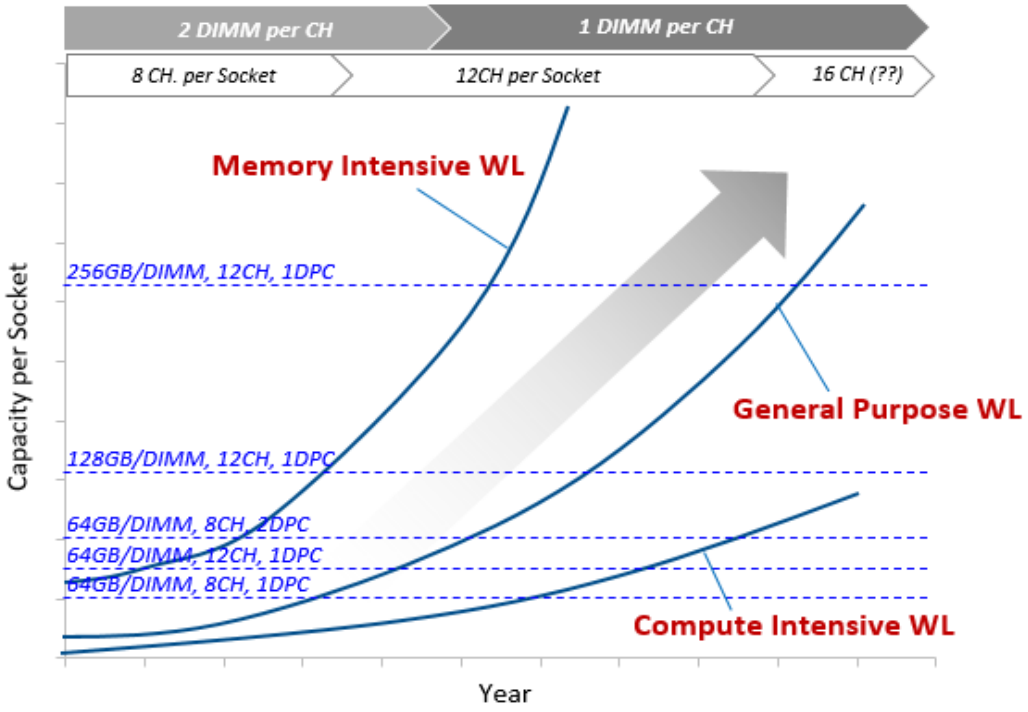
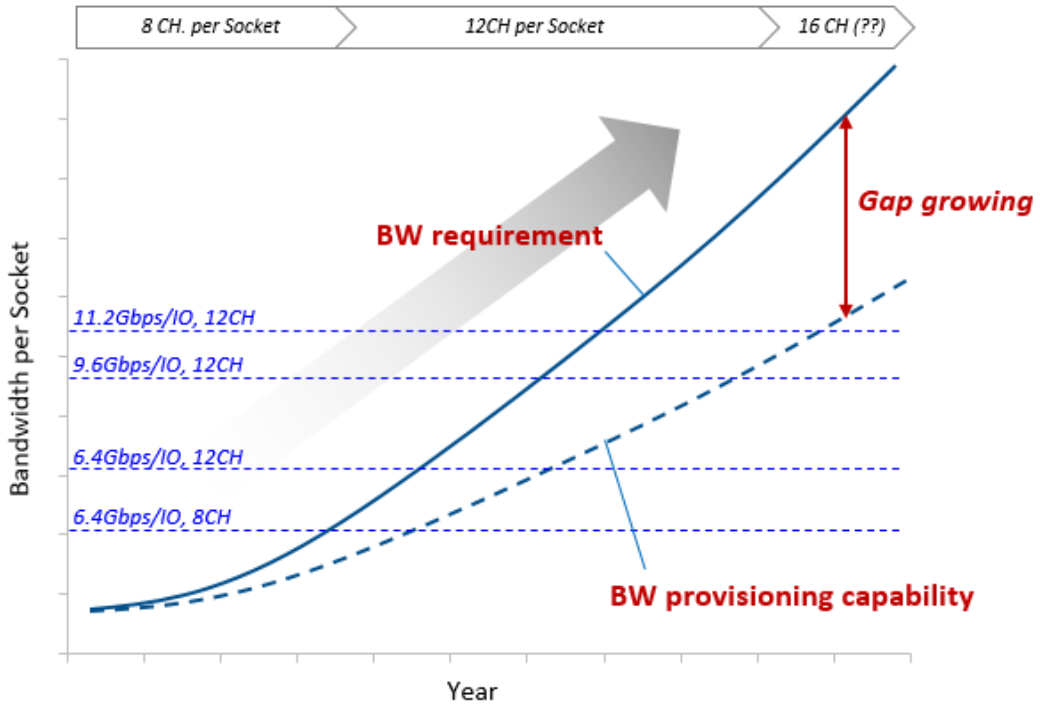
Growing Memory Bandwidth and Capacity Gap

- Increase in core counts requires continued increase in memory bandwidth and capacity
- Gap between such requirements and platform provisioning capability is growing
- CXL creates new opportunities beyond physical limitations, and enables efficient memory disaggregation



[Memory Capacity Requirement]

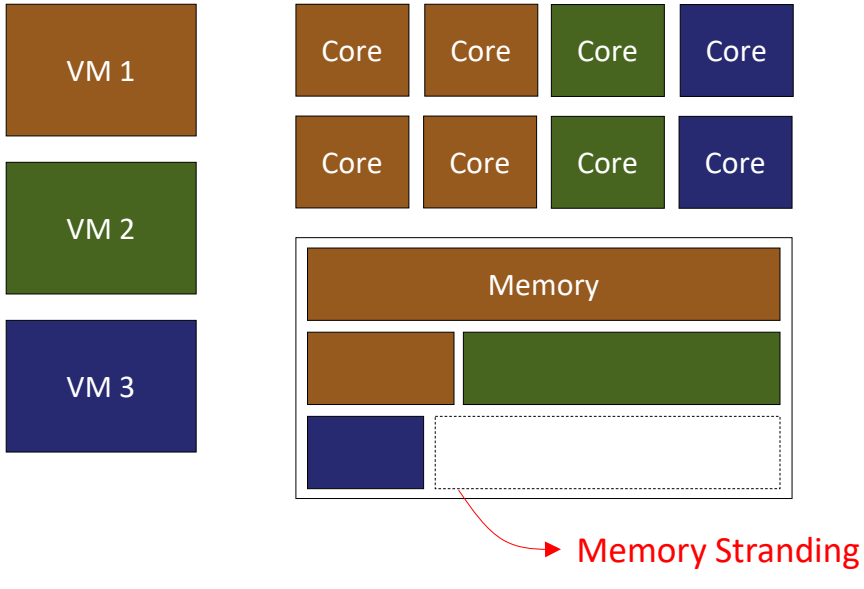


[Memory Bandwidth Requirement]

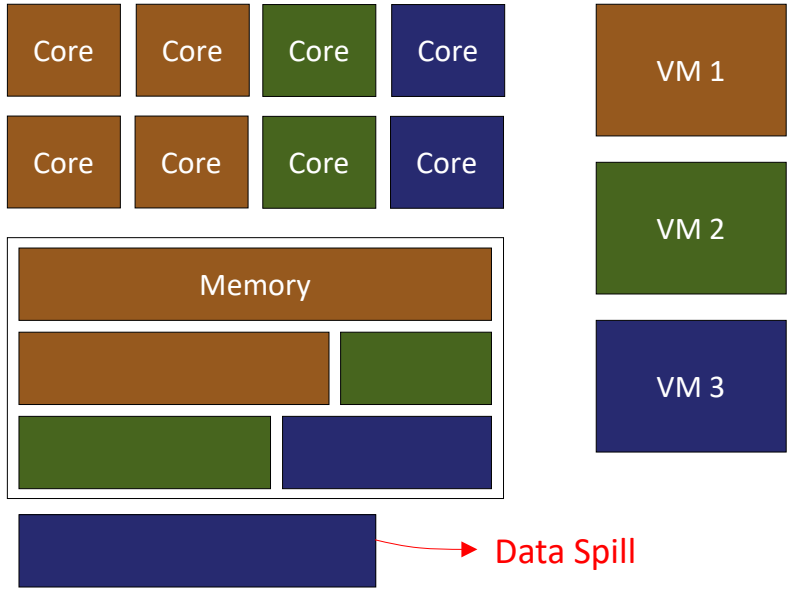
Challenges in Today's Datacenter

◯ Challenge 1 : Memory stranding and data spill

- Memory utilization of each node in a compute cluster varies time to time
- Unused memory in each node never be utilized by other nodes, which causes memory stranding and data spill



[Memory underutilization & Waste of memory costs]

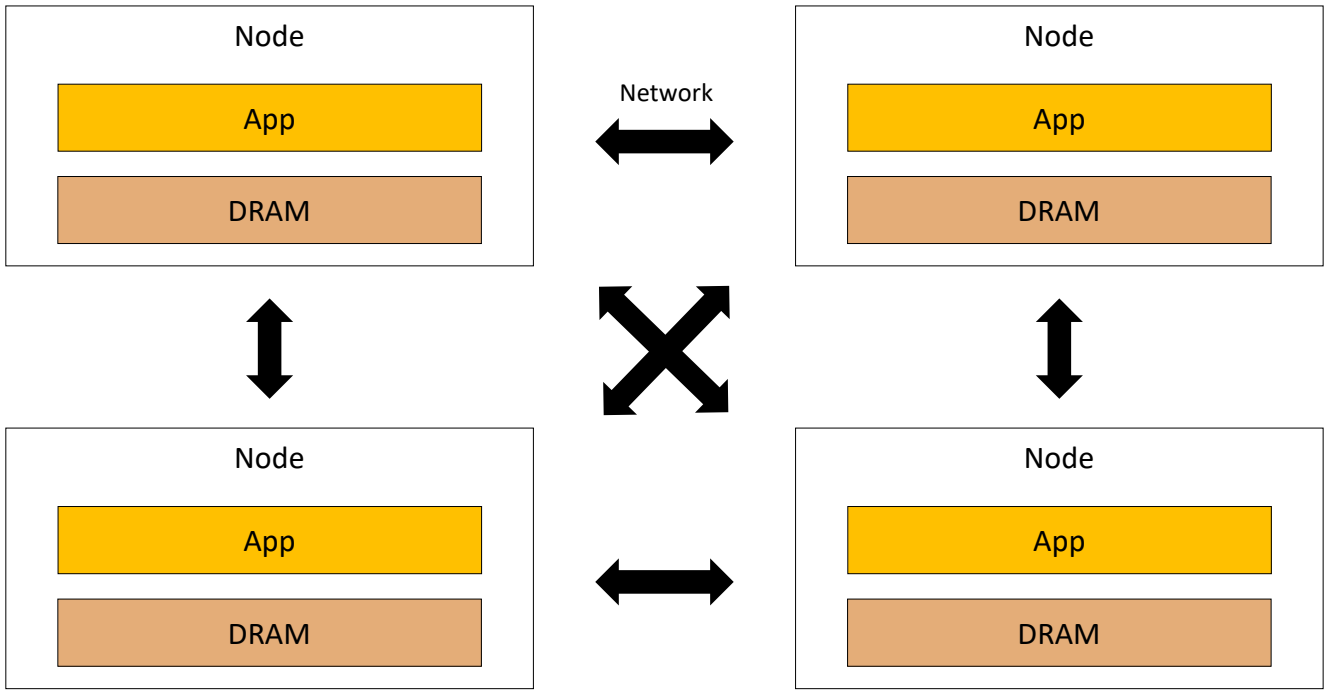


[Storage swap & Performance degradation]

Challenges in Today's Datacenter

◯ Challenge 2 : Data transfer overhead & data duplication

- In a distributed computing system, there is a network-based data transfer overhead between remote nodes
- Duplication of shared data between nodes increases local memory pressure



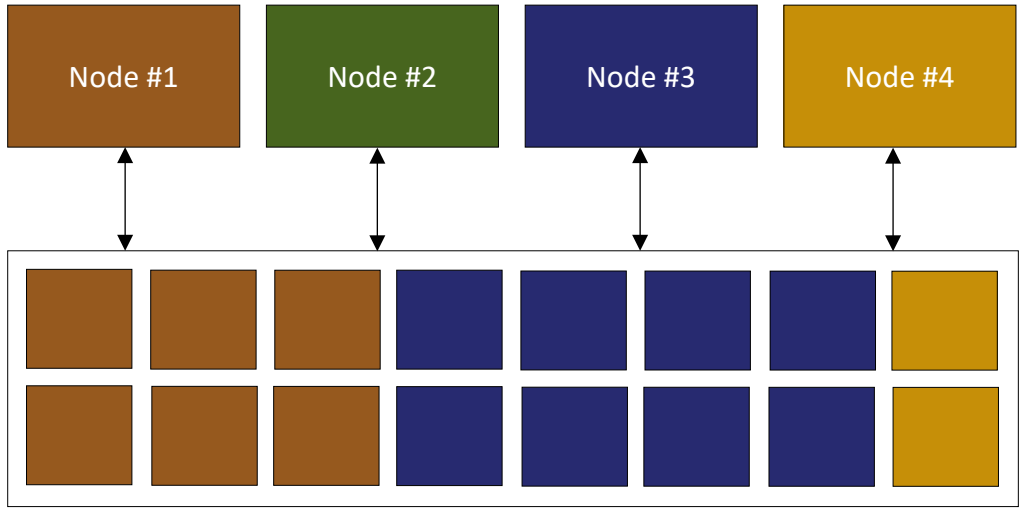
Serialization & Deserialization

Data Duplication

Solution: CXL Disaggregated Memory System

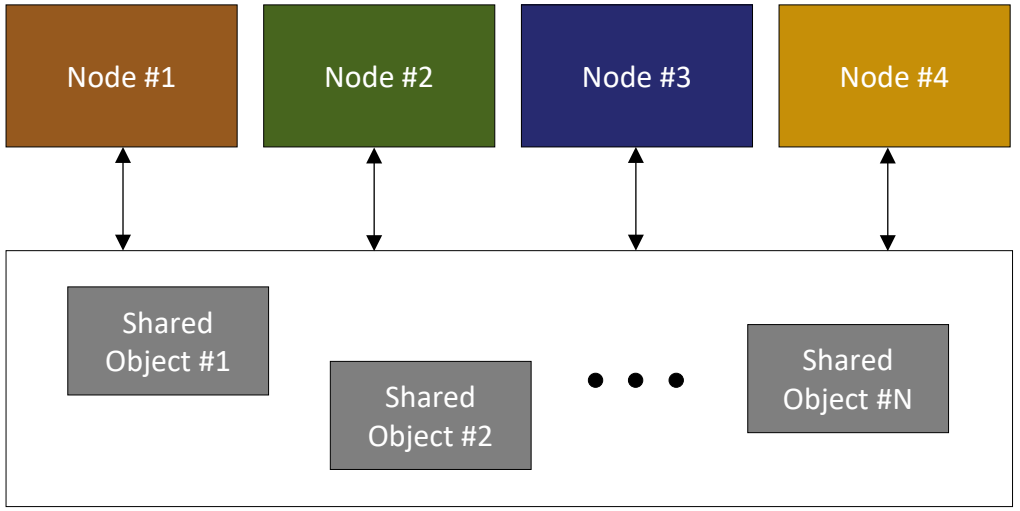
- **Support memory pooling and sharing with CXL disaggregated memory system**
  - **Memory pooling : Mitigate memory stranding and data spill by sharing memory resources between nodes**
  - **Memory sharing : Remove data transfer overhead and data duplication by sharing data between nodes**

Allocate CXL memory based on memory usage for each node



[Memory Pooling]

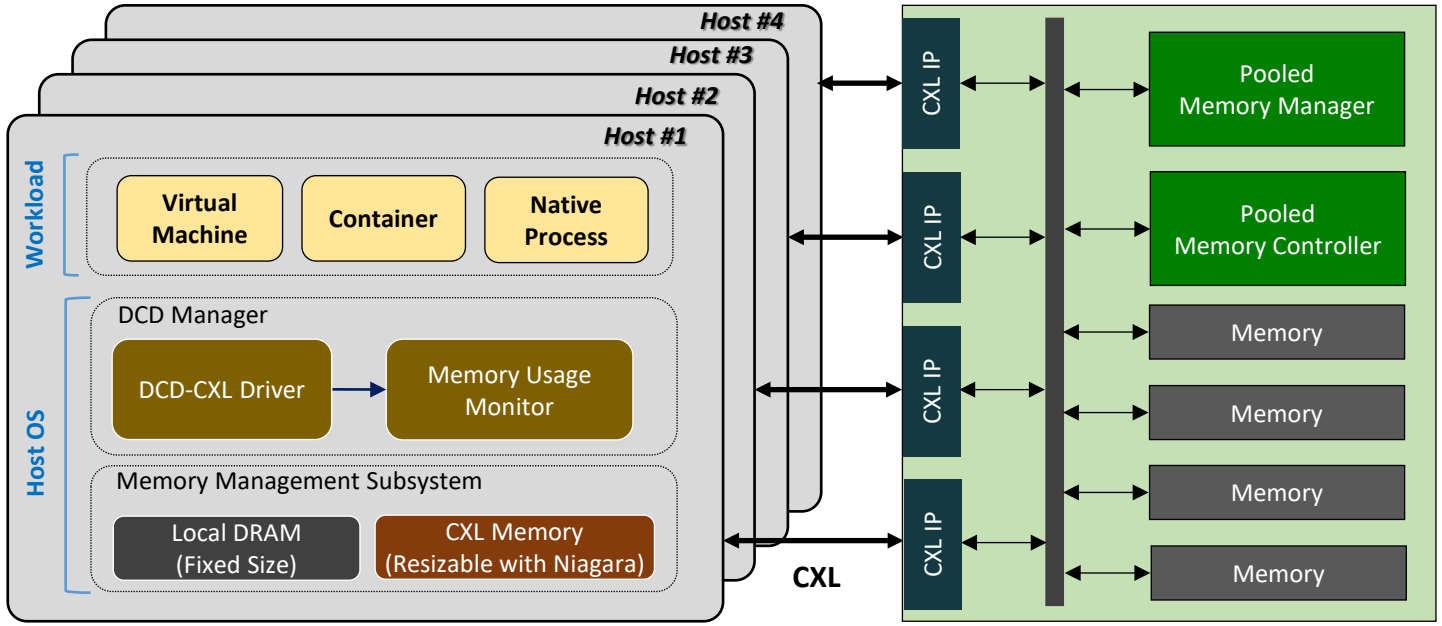
Share data objects based on zero-copy between nodes



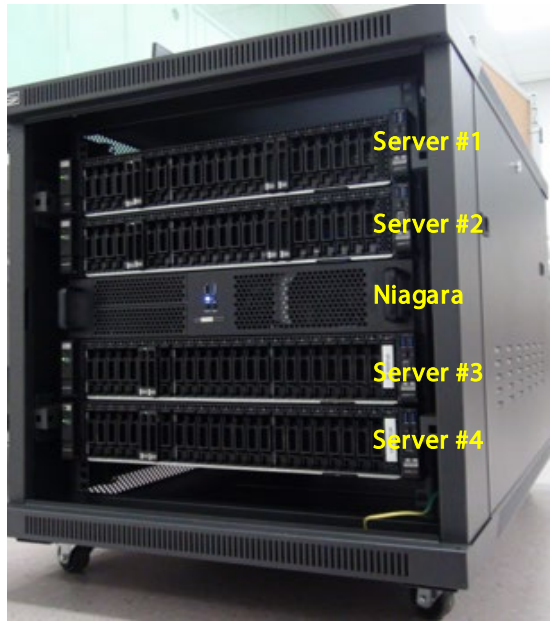
[Memory Sharing]

CXL Disaggregated Memory Research Platform

- **Built a Niagara HW/SW Research platform, an FPGA-based MH-SLD type of CXL disaggregated memory prototype, for memory pooling and sharing usage exploration**
  - **2U memory appliance which can connect up to 8 CXL host servers (without CXL switch)**
  - **Supports up to 4 channels of DDR4-DIMM (1TB)**
  - **Supports DCD (Dynamic Capacity Device) feature defined in CXL specification 3.1**

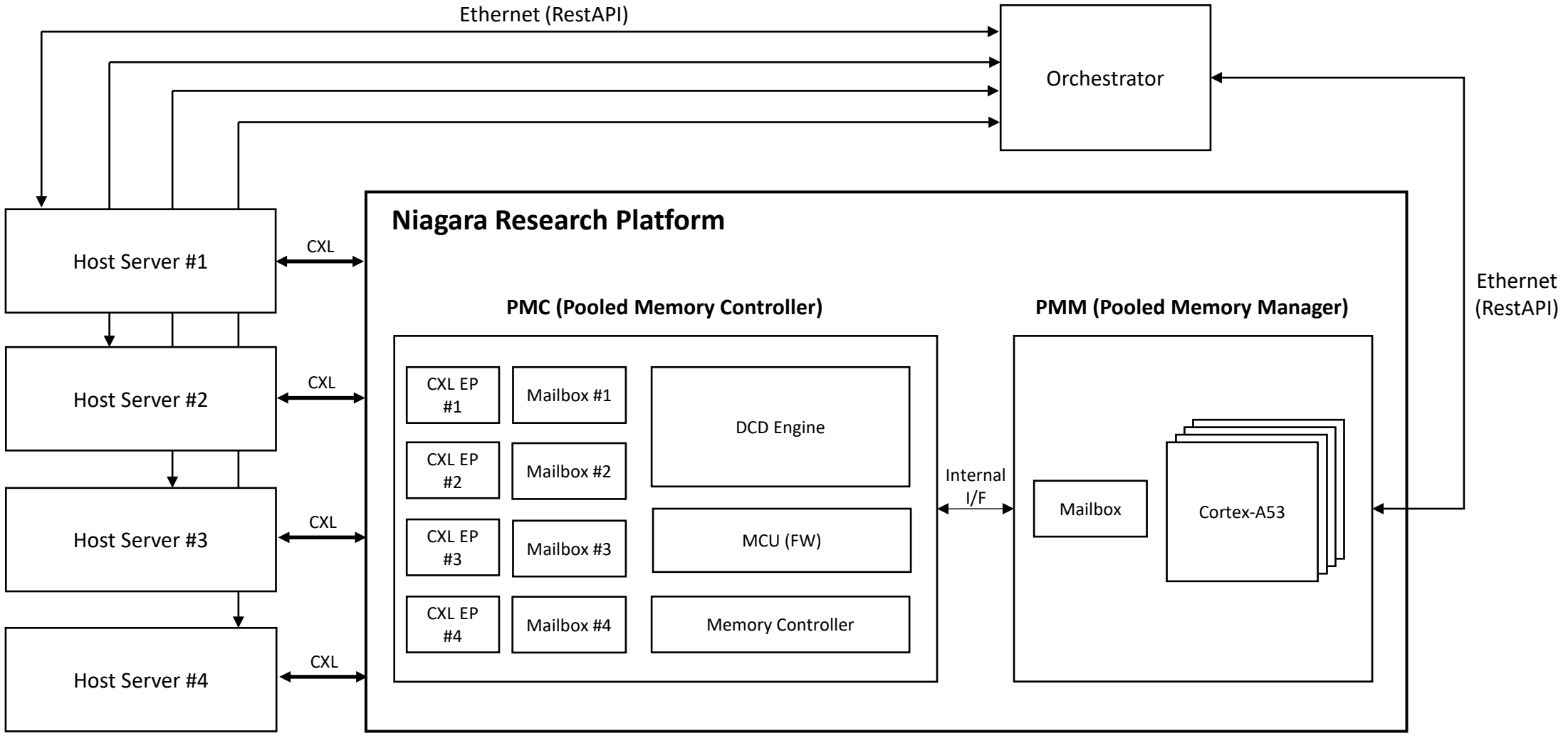


[Niagara HW/SW Research Platform]



[Rack-Scale System with Niagara]

DCD-Enabled Infrastructure

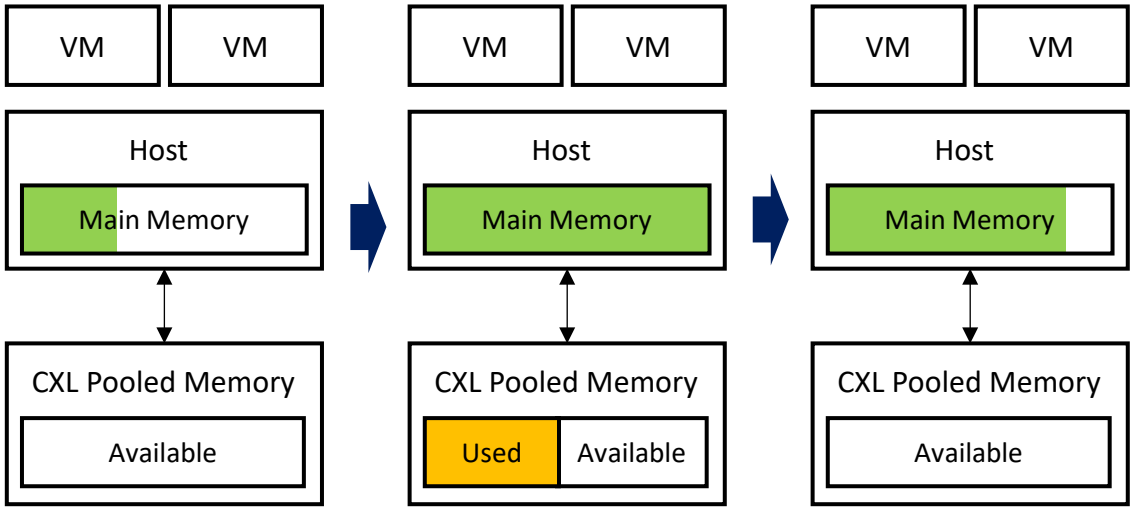


* Niagara supports DCD APIs defined in the CXL specification 3.1

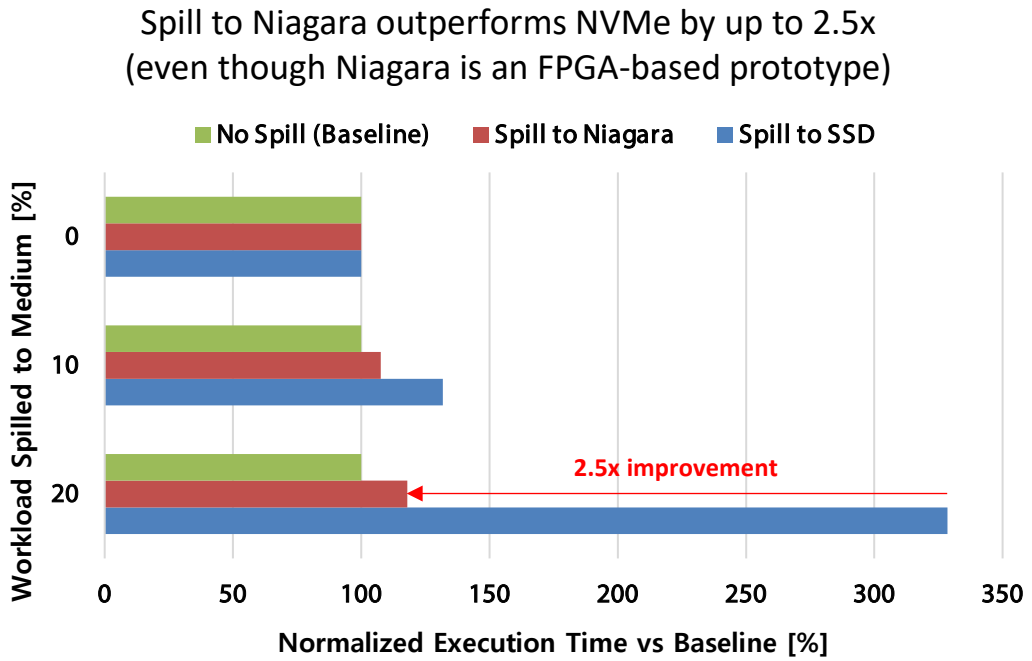
Use Case of CXL Disaggregated Memory

○ Use Case 1: Memory Pooling (Collaborate with MemVerge)

- Niagara can dynamically allocate/deallocate disaggregated memory resources for each node without RESET
- Improve memory utilization and performance of a system equipped with CXL disaggregated memory



[Memory Pooling without Workload Interruption]

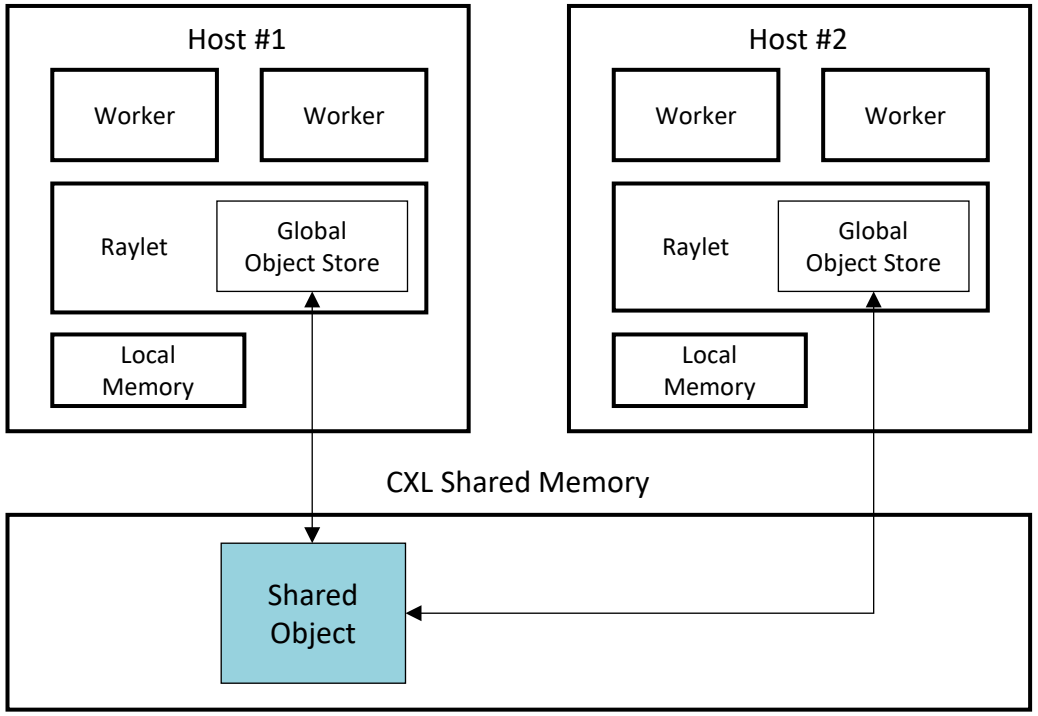


[Execution Time of CloudSuite In-Memory Analytics Benchmark]

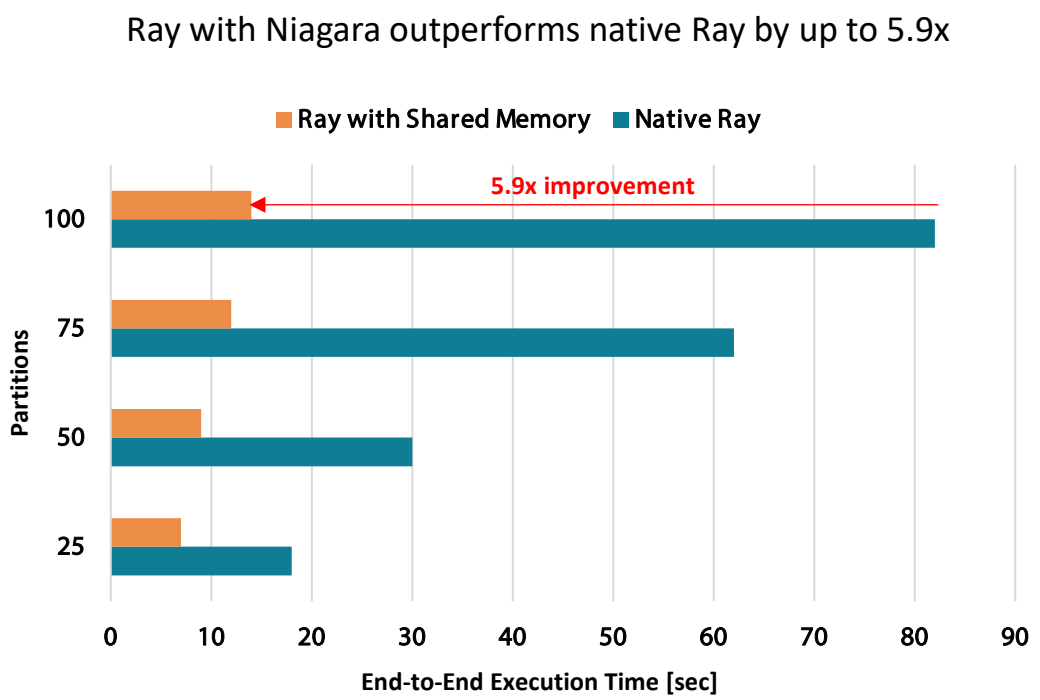
Use Case of CXL Disaggregated Memory

○ Use Case 2: Memory Sharing (Collaborate with MemVerge)

- No more object serialization and transfer over network for remote object access
- No more duplicate object copies on different nodes → zero copy



[*Ray-based AI/ML System using CXL Shared Memory]



[Execution Time of Ray Shuffle Benchmark]

*Ray is an open source based distributed computing framework for AI/ML

Future Work

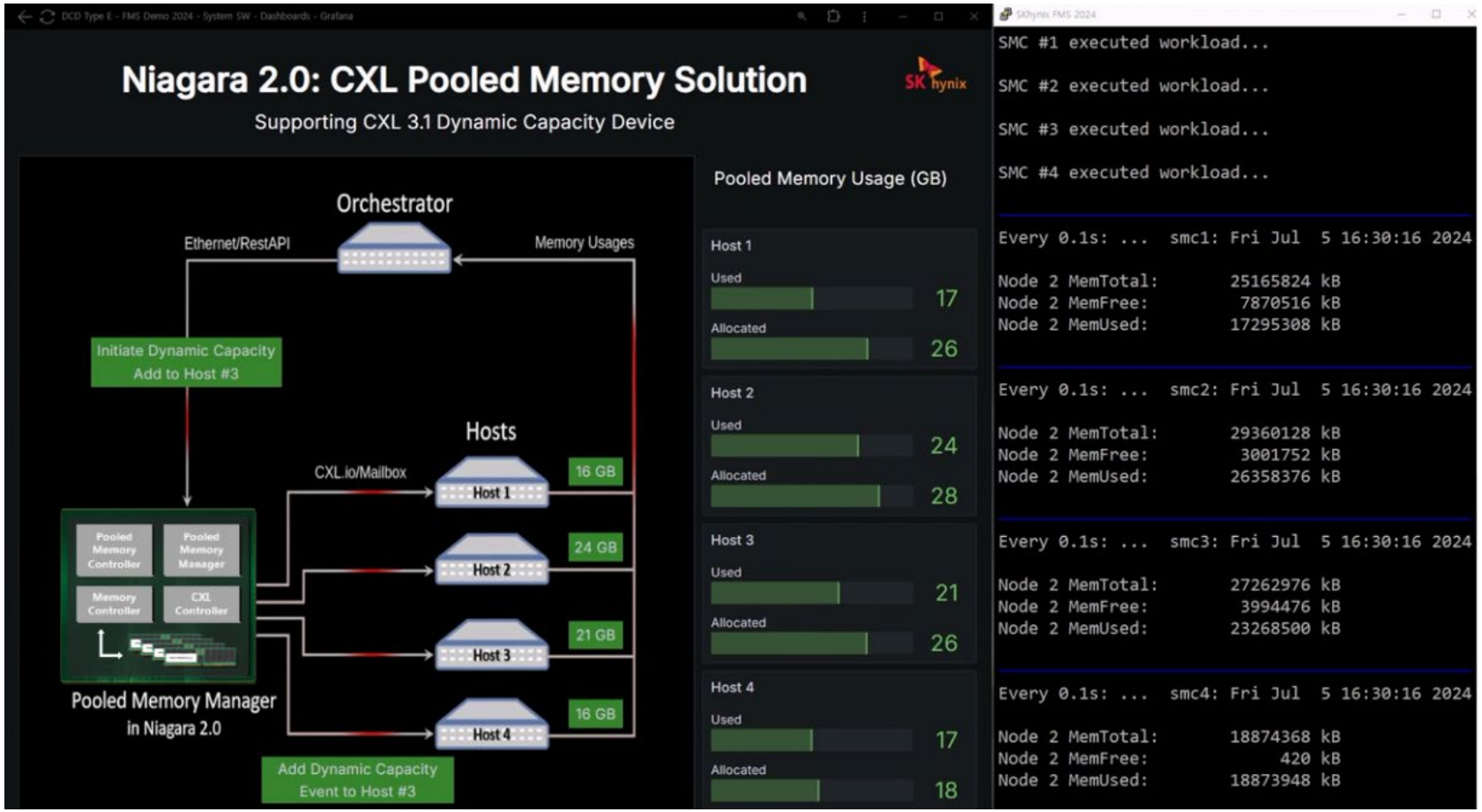
- **Research on Memory Sub-System Architecture based on Disaggregated Memory for AI Applications**
  - **System benefit for AI applications such as LLM (Large Language Model) and DLRM (Deep Learning Recommendation Model)**

- **Research on Value-added Function for Efficient Use of Disaggregated Memory**
  - **Near data processing**
  - **Telemetry (hotness tracking, average latency and throughput)**

We look forward to an open collaboration with industry partners to enable HW/SW ecosystem

Demo in SK hynix Booth #207

- **Demonstrate the memory resource allocation/deallocation of CXL disaggregated memory based on the dynamic changes of memory requirements from VM servers**



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