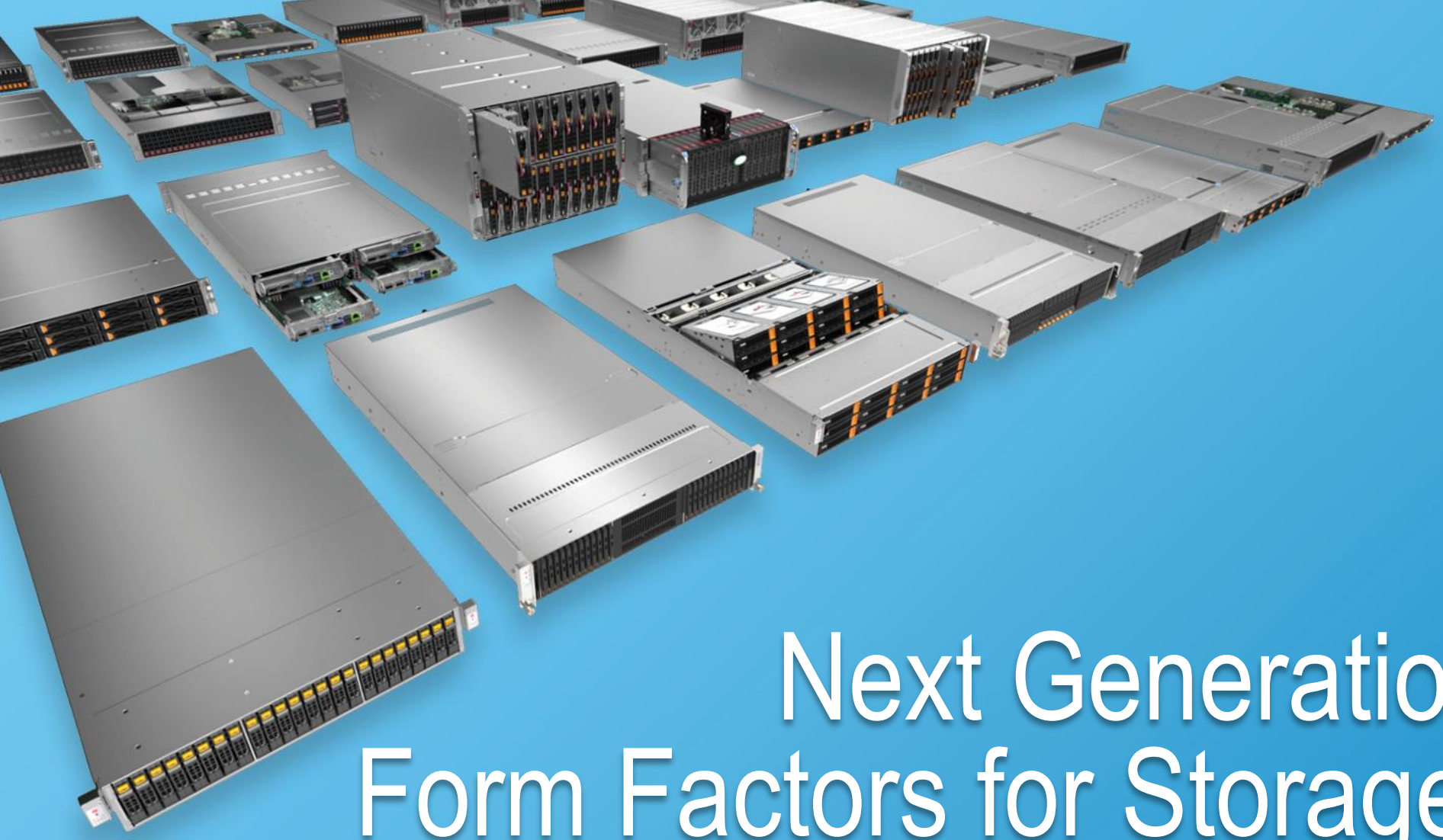


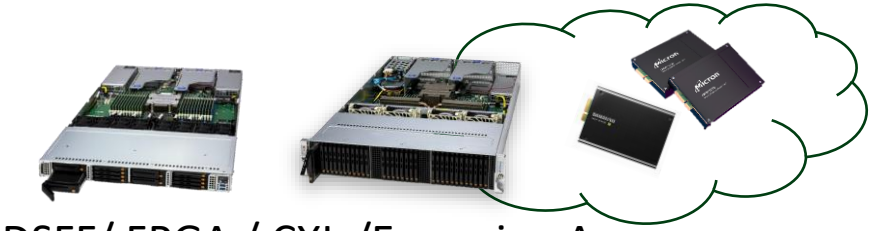
Paul McLeod

Director, Storage Systems

Supermicro

Next Generation Storage Form Factors for Storage Systems

Transitions in Storage System Architectures



EDSFF/ FPGA / CXL /Emerging Apps

PCIe Performance

SAS & SATA

NVMe/U.2

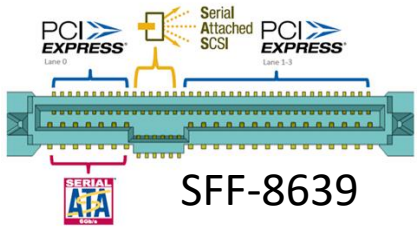
ESCON, FC, etc

Parallel SCSI

Parallel ATA

Serial Connectivity

SAS/SATA, U.2 & U.3/Tri-mode



SFF-8639

Single Fabric Vision

Cost / Compatibility

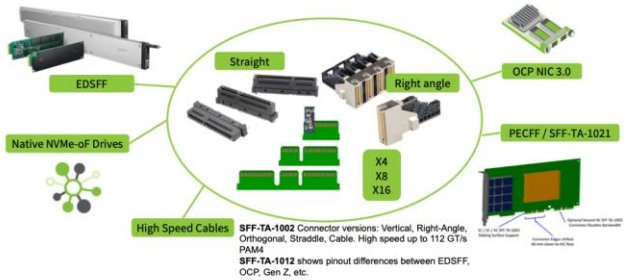
iSCSI, FCoE, Kinetic, Fabric attached Media, Etc.

2000 | 2010 | 2015 | 2020 | 2025

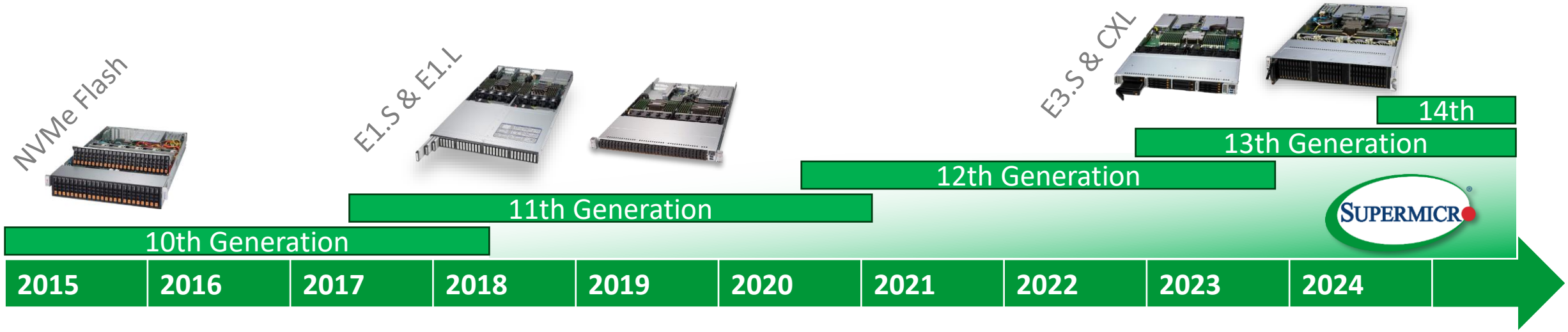
Embracing Emerging Standards

EDSFF and CXL

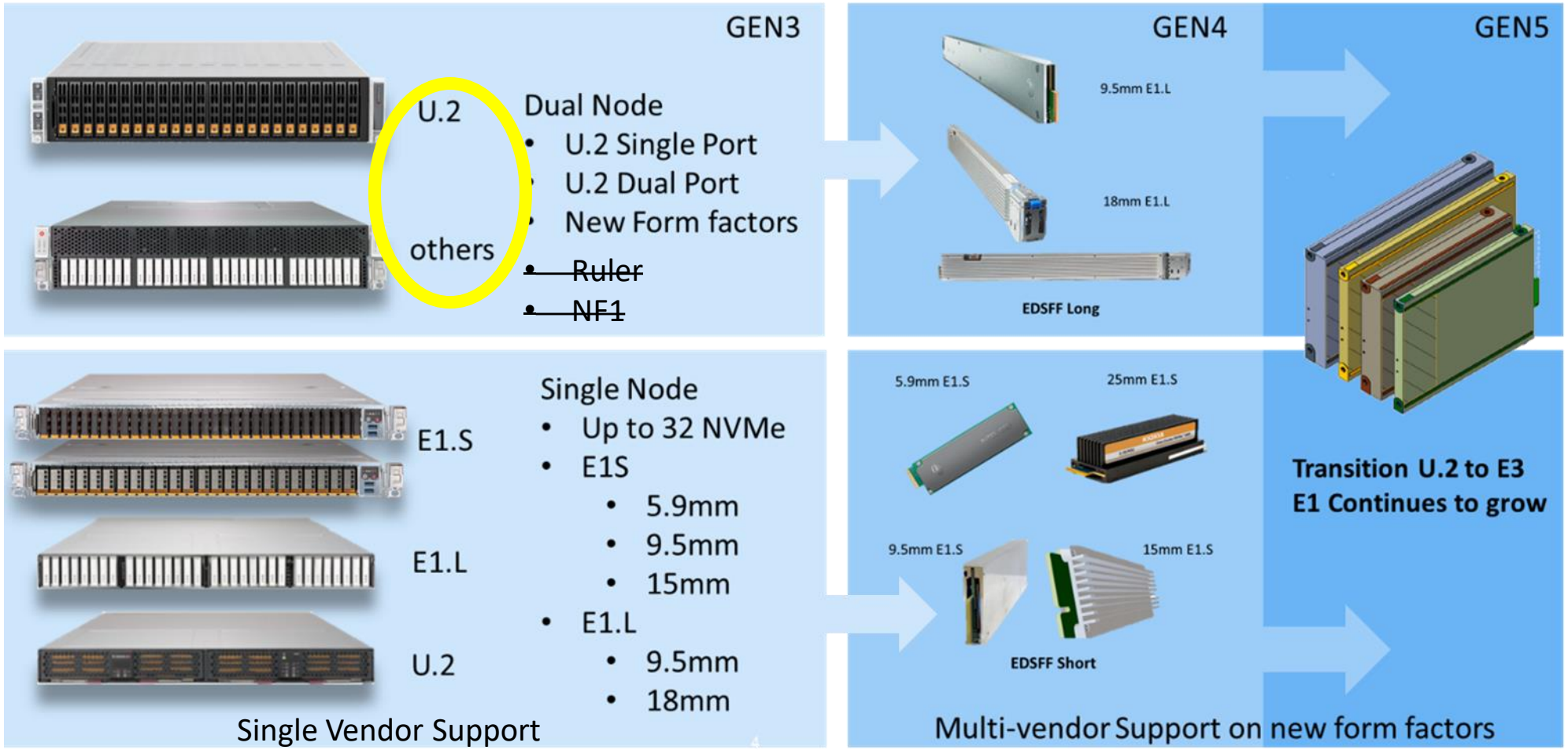
EDSFF E1.S, E3.S, and E3.L form factors, as well as AICs, have been integrated into the Compute Express Link® (CXL®) ecosystem, underscoring their utility in high-performance, high-capacity server environments promoting robust, scalable, and efficient designs.



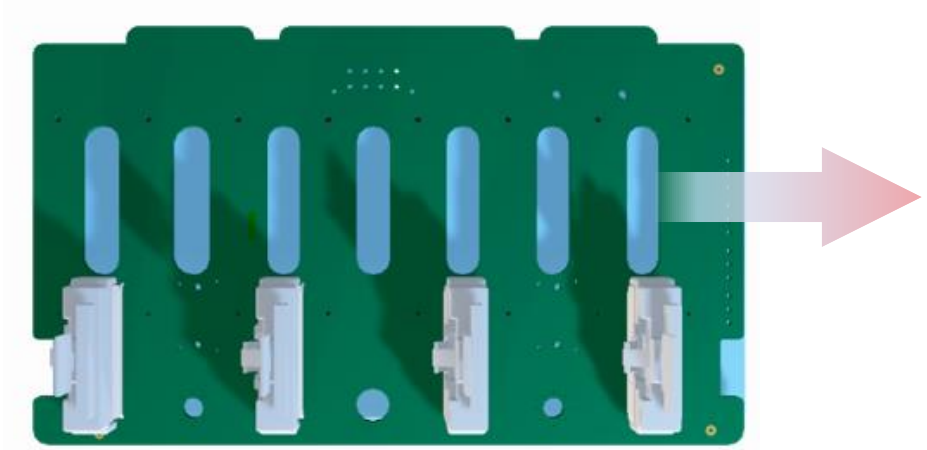
Source: SNIA



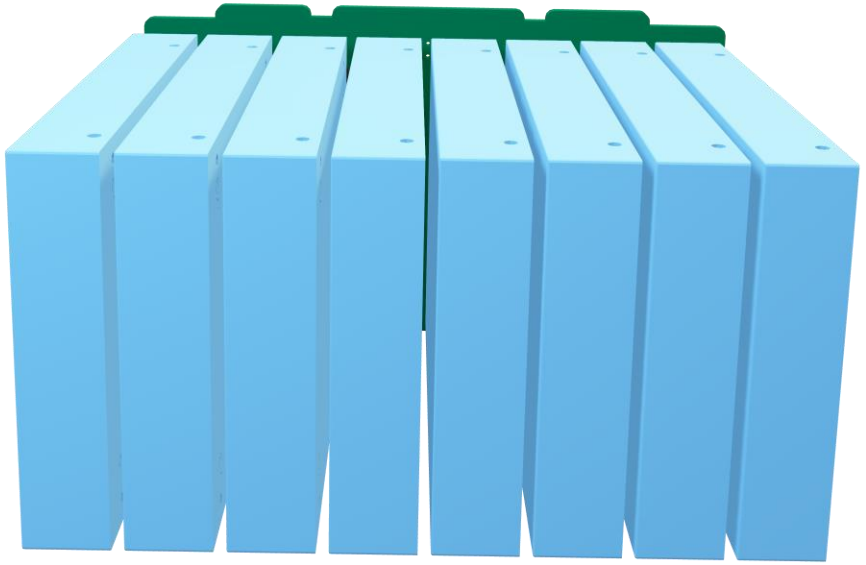
Supermicro and storage form factors

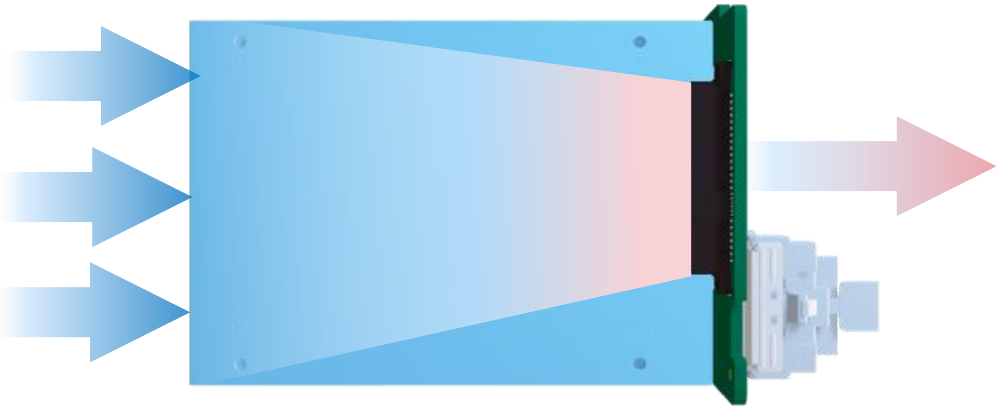


Legacy Storage Bay Design (U.2)

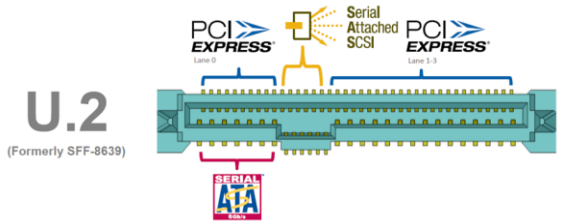


Traditional backplane design limits airflow



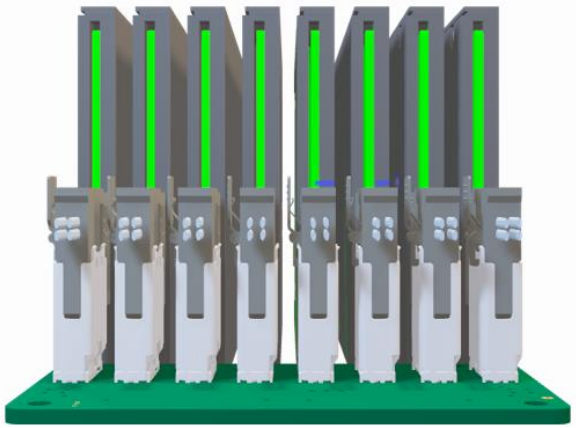


PCBA trace limits PCIe bay definition in manufacture

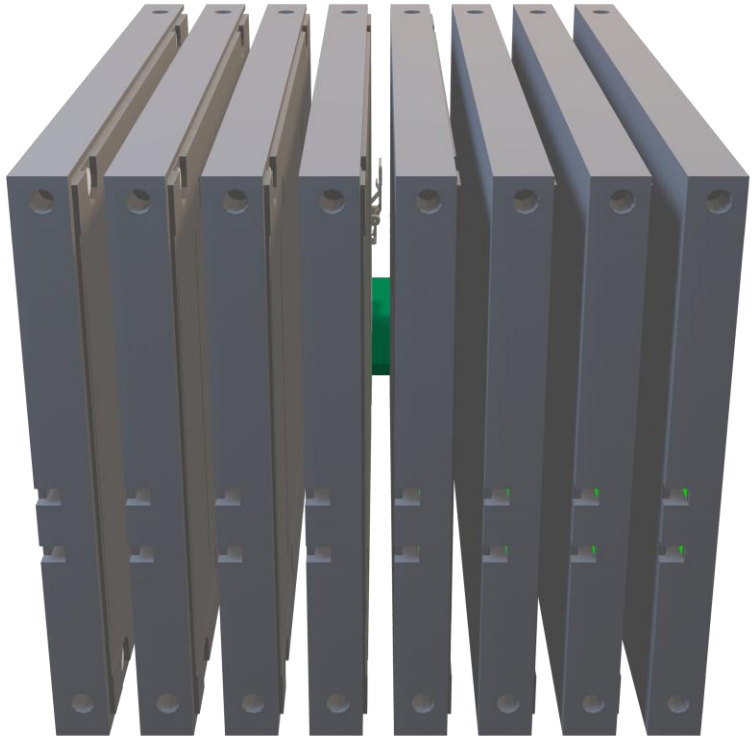


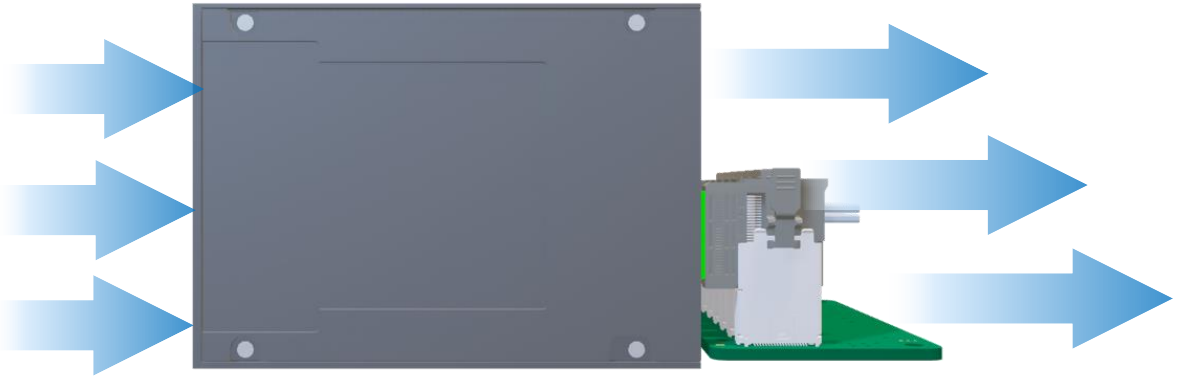
The SFF-8639 drive connector has served the Industry very well and will continue for the foreseeable future!

EDSFF Storage Bay Design (E3.S)



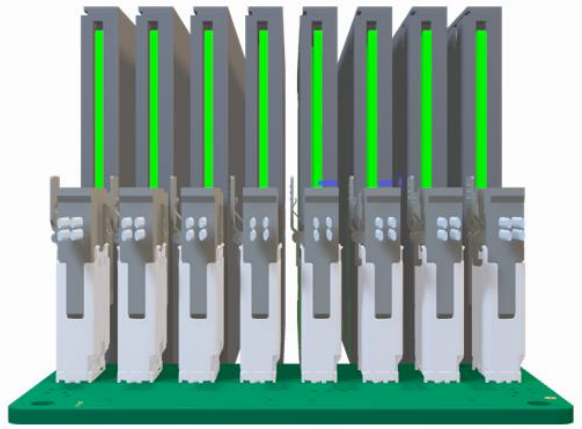
EDSFF bay design optimizes airflow

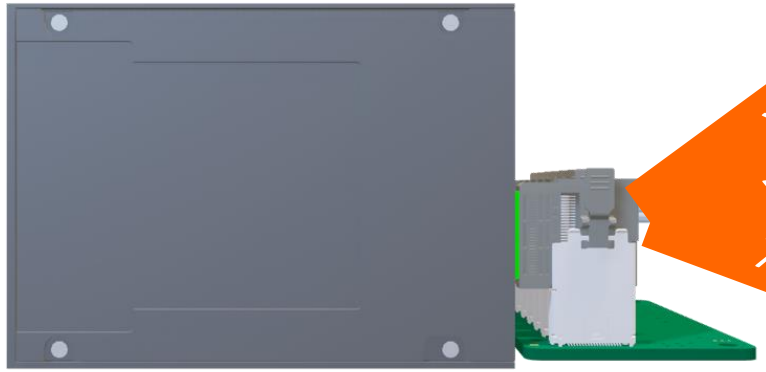




Power, and device/bay management are the only traces on the PCBA

EDSFF Storage Bay Design (E3.S)





Backplane traces: Power and device management

EDSFF building blocks allows for the change of PCIe lanes to the media/bay by changing a cable!

X8 cable

X4 cable

X2 cable

X8 PCIe Lanes

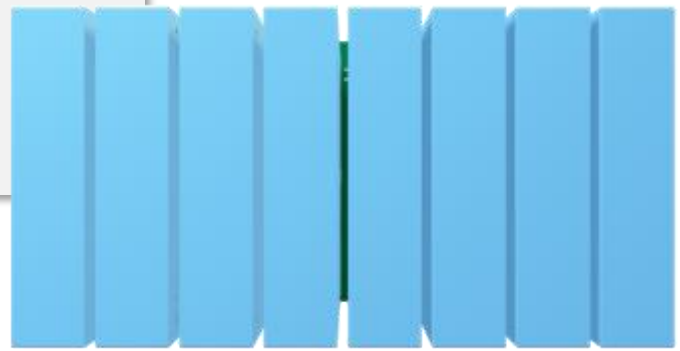
X4 PCIe Lanes

X2 PCIe Lanes

Gen5 EDSFF Petascale Platform Innovation

- **Superior Signal Integrity**
  - Mainboard direct connection to SFF-TA-1002 1C connectors/SSDs and reduce the backplane routing signal loss
  - Reduce ~40% of the signal loss
- **Better Air Flow**
  - No vertical backplane blocking the air flow
  - ~ 75% increase in front opening
  - ~ 20% improvement system CFM

E3.S SSD + EDSFF BPN



U.2 SSD + BPN

Gen5 EDSFF Petascale Platform Innovation

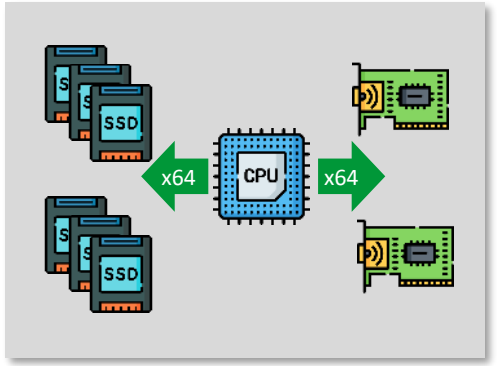
Purposed Built for New All-NVMe and Software-Defined Data Center

- **Unified Chassis**
  - Support
    - Intel DP and AMD UP
    - 1U up to 24 E1 SSD
    - 1U up to 16 E3 SSD and CXL
    - 2U up to 32 E3 SSD
  - Less than 31” chassis depth

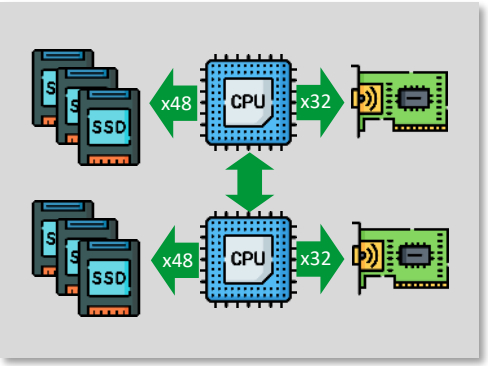
- **Balanced Architecture**
  - Front storage IO and rear networking
  - Simplify’ s NUMA, IO complexity

< 31” chassis depth

1U16, 1U24, 2U32 and CXL



AMD Single Processor



Intel Dual Processor

X13 & H13 Petascale All-Flash Highlight

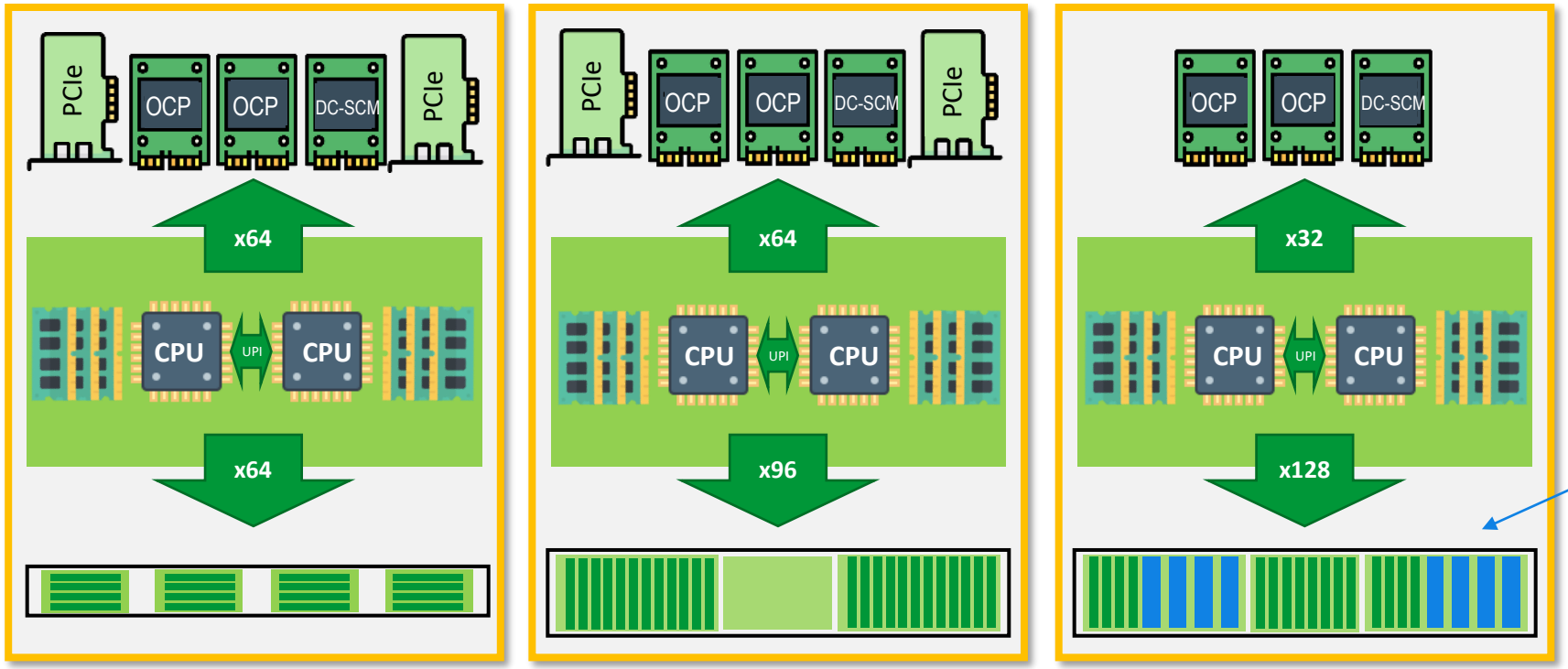
- **Key Features**
  - Support dual Intel and single AMD single PCIe Gen5 Processor
  - Support 1U E1.S and E3.S and 2U E3.3 TLC, QLC and CXL device and up to 1PB all flash in 2U
  - Optimized thermal design with EDSFF design
  - Balanced PCIe lanes for front SSD and rear IO design
  - Up to 30M 4KB RR IOPS and 230+ GB/s 128KB SR BW.

- **Target Solutions**
  - High performance AI SDS building blocks
  - Virtualization & dense VDI
  - High performance object storage
  - Hyperconverged infrastructure
  - High performance CDN and video streaming

NEW!

X14 Petascale Flexible Topology (DC-MHS)

Providing Balanced Storage and Networking Bandwidth in 1U and 2U Enclosure Design



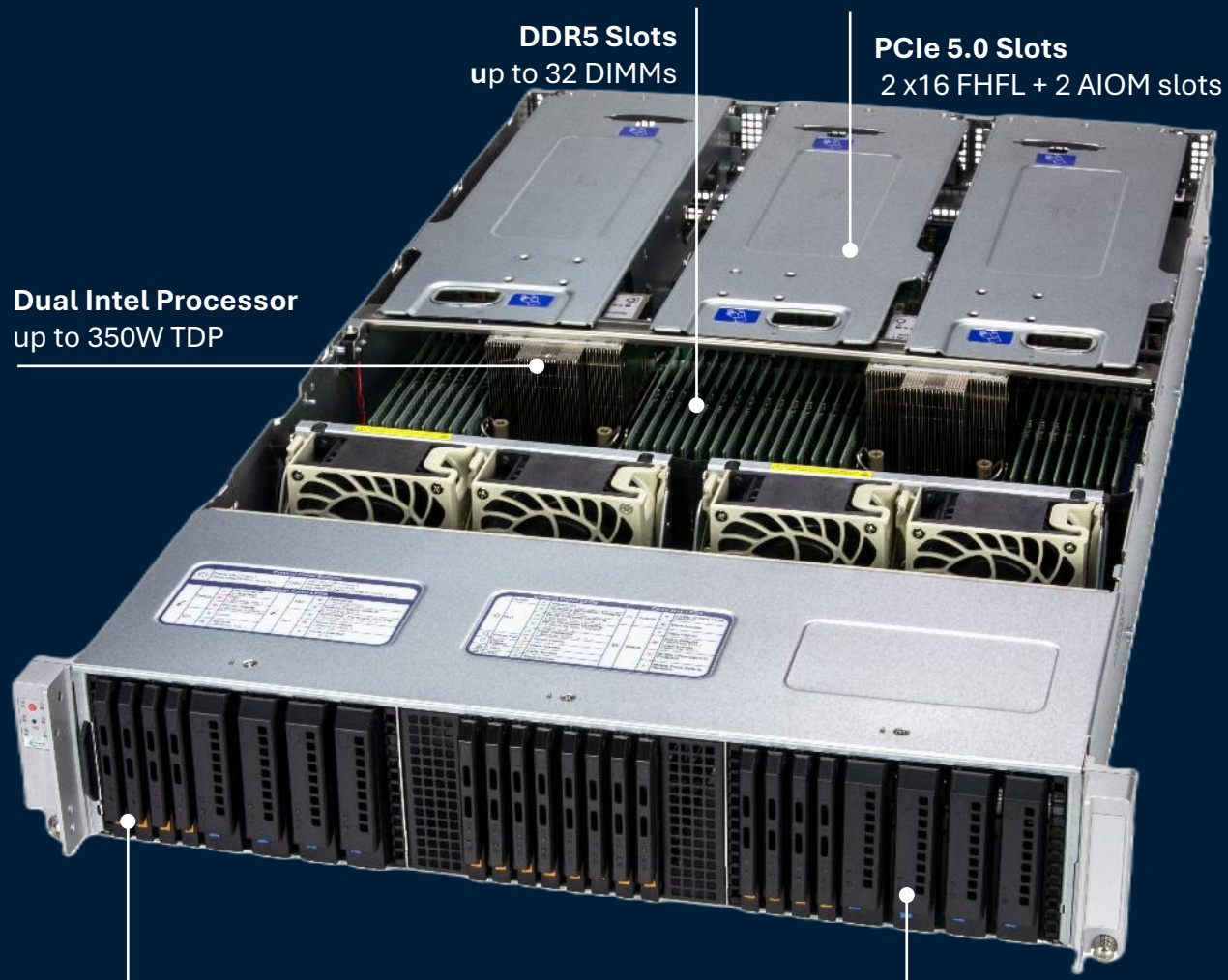
1U/16 E3.S SSD (x4)

2U/24 E3.S SSD (x4)

2U with 16 E3.S SSD (x4) and 8 E3.S 2T CXL (x8)

New!

X14 2U24 EDSFF E3.S & CXL Petascale Storage (DC-MHS)



CXL (Type 3) Memory Expansion Use Cases

Capacity Expansion

- Adding memory while not adding server
- Memory capacity centric workloads (IMBD)

Bandwidth Expansion

- Performance improve by aggregate memory BW
- Memory BW centric workloads (AI)

Capacity and Bandwidth Expansion

- Combine #1 and #2 requirements
- Perf centric workload, Inference and LLM etc workloads

Tiered Memory

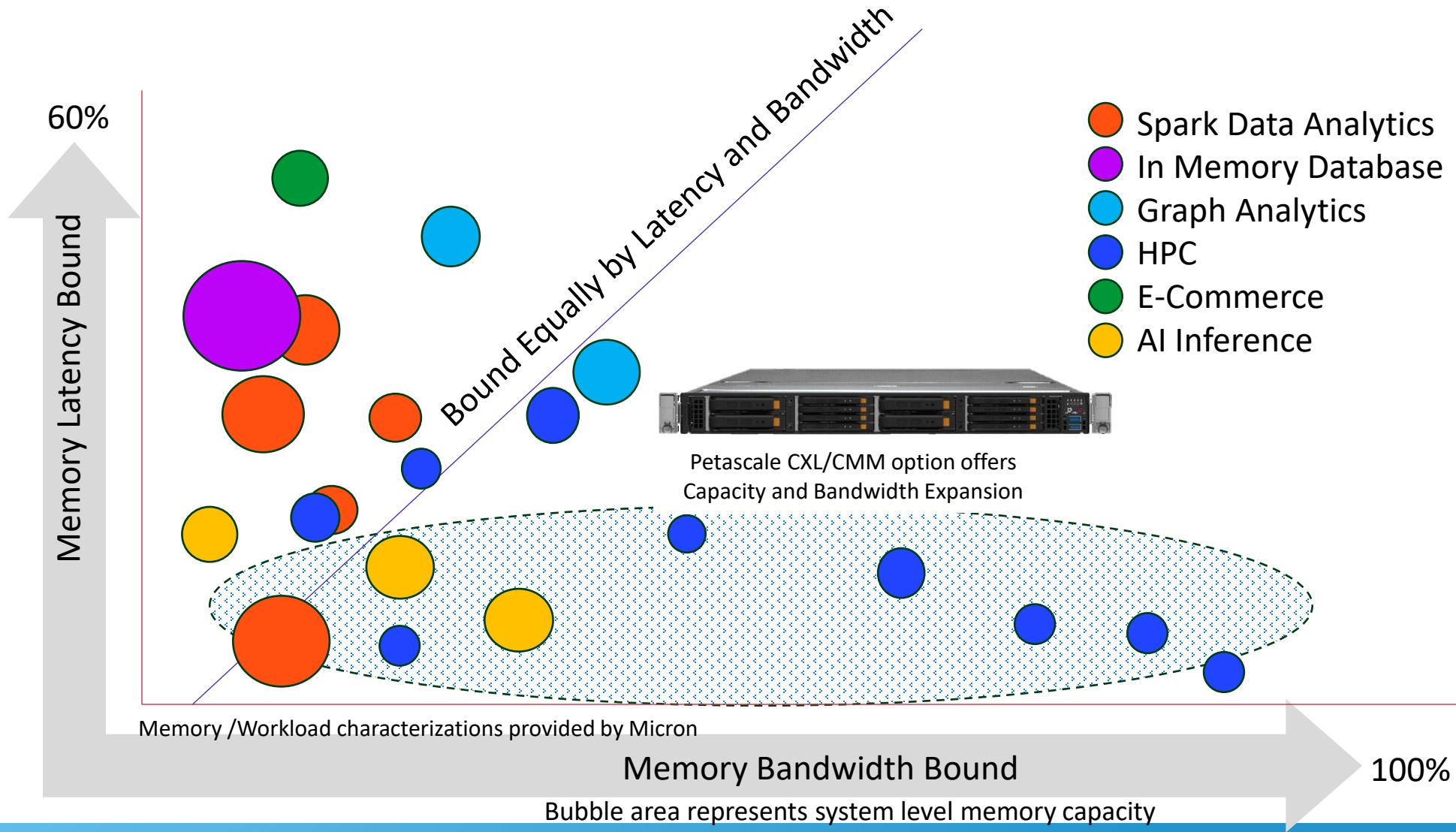
- Limited increase capacity/bandwidth w/ low cost CXL
- Tiering workloads (hot/cold tiering)

Memory Pooling

- Dynamic memory allocation in rack level
- Reduce DC or Rack TCO but increase latency

New CXL Memory Expansion Helps Data Center to Lower the TCO

Memory Workload Characterization



CXL Features Over Generations

CXL 3.0 Spec Feature Summary

Features	CXL 1.0 / 1.1	CXL 2.0	CXL 3.0
Release date	2019	2020	1H 2022
Max link rate	32GTs	32GTs	64GTs
Flit 68 byte (up to 32 GTs)	✓	✓	✓
Flit 256 byte (up to 64 GTs)			✓
Type 1, Type 2 and Type 3 Devices	✓	✓	✓
Memory Pooling w/ MLDs		✓	✓
Global Persistent Flush		✓	✓
CXL IDE		✓	✓
Switching (Single-level)		✓	✓
Switching (Multi-level)			✓
Direct memory access for peer-to-peer			✓
Enhanced coherency (256 byte flit)			✓
Memory sharing (256 byte flit)			✓
Multiple Type 1/Type 2 devices per root port			✓
Fabric capabilities (256 byte flit)			✓

Not supported

✓ Supported

Intel : 5th Gen Xeon
AMD : Genoa & Bergamo

Intel : Xeon 6
AMD : Turin

Micron CXL CZ120 Partnership and Seeding Program

Supermicro in Partnership with Industry Leading Technology Companies Delivering Early Access to CXL

Introducing Micron CZ120 Memory Expansion Modules

Delivering capacity, bandwidth, flexibility

128GB / 256GB

Up to 2TB incremental server capacity[1] supporting CXL 2.0

Up to 36GB/s[2]

Up to 24% increased server memory read/write bandwidth[3]

E3.S 2T PCIe Gen5 x8

Industry-standard form factor for broad deployment

1. By adding 8x256GB CZ120s, system limitations may apply.
2. Measured by running MLC workload with 2:1 read/write ratio on a single CZ120 module.
3. MLC bandwidth using 12-channel 4800MT/s RDIMM + 4x256GB CZ120 vs. RDIMM only.

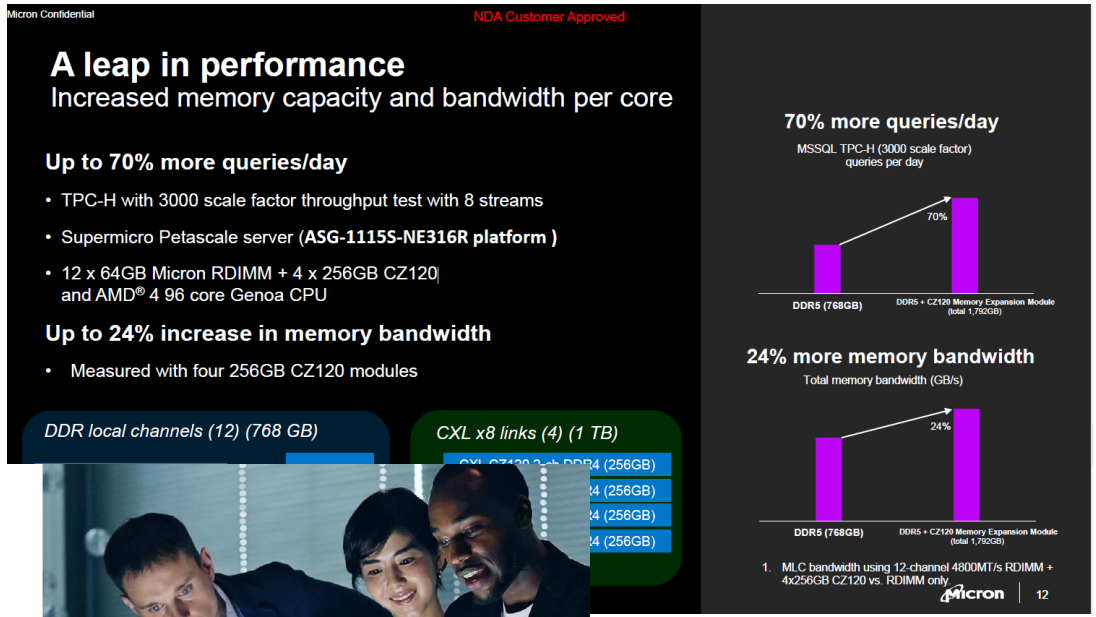
Micron Technology Enablement Program (TEP)

Cloud Service Providers, Original Equipment Manufacturers and Original Design Manufacturers — Qualify our CZ120 into your server platforms by enrolling with Micron TEP

Hands-on support to aid in the development of CXL™-enabled designs

- Technical resources including data sheets, electrical and thermal models to aid in product development and evaluation, and engineering consultation related to signal integrity and other technical support topics
- Access to other ecosystem partners who can aid in system-level design

Learn more micron.com/CXL



EDSFF - High Efficiency by Design

- Increasing CPU Cores & PCIe Lanes = *More capabilities*
- Memory Capacity & Bandwidth with CXL= More performance tiers
- Direct Attached EDSFF Bays = *Lower latency*
- Better Air-flow = *Better power efficiency*
- Better Signal Integrity= *More IOPS*

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