SPI NAND Flash Octal DDR Verification

Challenges and Solution

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Introduction

- To meet the increasing bandwidth needs of the automotive industry, SPI NAND Flash memories have evolved from a 1-bit slow clock SPI interface to fast clock speeds over 2-bit and 4-bit SPI interfaces
- Recently memory vendors added the Octal SPI interface that enables 8-bit wide high bandwidth synchronous data transfers at manageable clock speeds
- In several cases, the Octal SPI interface is combined with double data rates (DDR)
- The Octal double data rate protocol uses a byte-wide synchronous bus interface on both rising and falling edge of the clock for command, address and data
- Winbond's Octal DDR is further combined with high speed continuous read across Page and Block boundaries
  - Offers a fully integrated on-chip solution for high speed read
  - BUT increases the complexity of the verification matrix

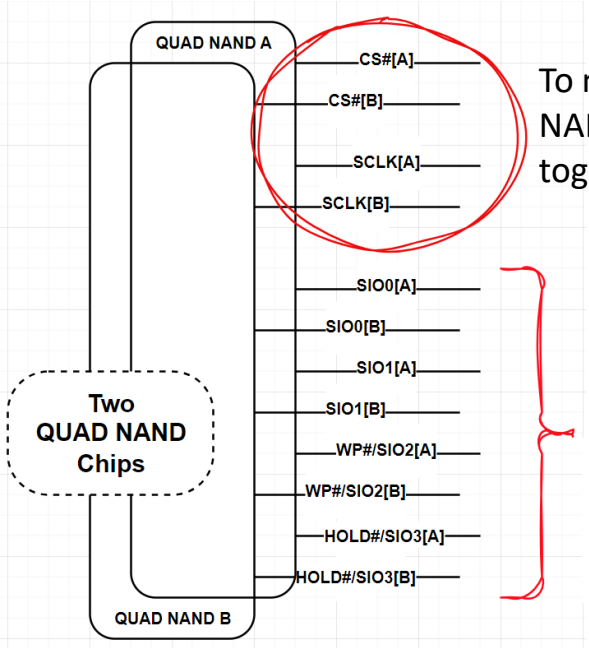
Motivation for SPI Octal NAND: Winbond perspective

- Emerging Automotive applications require high-density/high-performance Code Storage Flash
- Most of these applications emerged in past 5~10 years, with some of examples below:
  - Advanced FCM “Front Camera Module”: 1Gb~4Gb Flash, < 10 sec startup time
  - DMS “Driver Monitor System” (Europe passed requirement, others to follow): 1Gb~2Gb, 5~10 sec startup time
  - Domain control for Surround View System and auto-parking: 1Gb~2Gb Flash, rear camera < 2 sec (NHTSA/USA)
- Winbond introduced W35N01/02/04JW Octal NAND at 240MB/s to meet these requirements
  - Octal NAND at 240MB/s (120MHZ Octal DDR with DS “Data Strobe”) can download 2Gb in mere 1 sec
    => QspiNAND at 80MB/s (80MHZ Quad DDR) downloads 2Gb in 3 sec, decent but too long for some applications
- New solution of Octal NAND to address whole eco-system: SoC, EDA, customer SW
  - SoC partners have enabled or are in process of enabling support for Octal NAND
  - EDA partners such as Cadence provide timing models (covered in paper) to help with SoC support of Octal NAND
  - SW support such as for low-level drivers, linux and Autosar should be available for end customers, as needed
- With many projects in production and under design, SPI Octal NAND is rapidly proliferating

Problem Statement

- NAND Flash devices have a higher memory density compared to alternatives such as NOR Flash
- Device of choice for the new era of high-capacity storage Automotive application space
- But changes in architecture and design implementation present validators with limited options for rapid and effective verification
- The Octal SPI interface is intentionally pin compatible with Octal SPI NOR Flash devices, but the existing verification memory models for NOR Flash devices cannot model the Serial NAND Flash memory architectures and addressing
- The Serial NAND Flash verification memory models currently available in the market are x1, x2, or x4 SPI Quad NAND devices
- While these could mimic the SPI NAND devices architecturally, they cannot model the Command-Address-Data instruction sequences at the transactional level
- A user cannot connect multiple copies of the SPI or SPI Quad NAND devices to try and mimic an Octal device –
  - The signaling is incompatible
  - AC/Timing parameters vastly inaccurate compared with actual SPI Octal NAND Flash devices

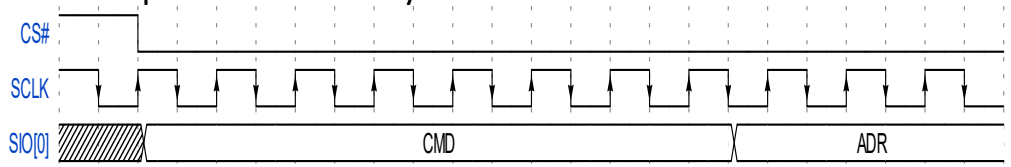
Case in hand: NXP ODDR Verification



To mimic a single Octal DDR SPI Serial NAND device, could tie the **CS#** pins together and the **SCLK** pins together

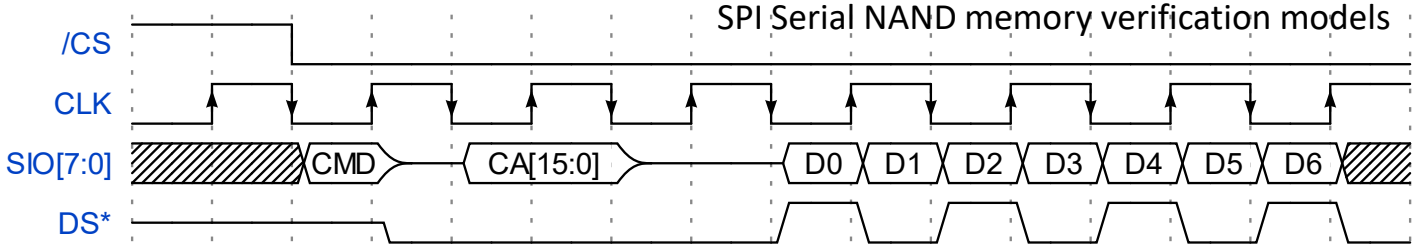
There would be 8 **SIO*n*** pins for the 8-bit Octal controller - But the command-address-data encoding scheme would be completely broken regardless of how the pins are interleaved in the testbench

The SPI Serial NAND device can only receive command on **SIO0** pin over 8 clock cycles for 8-bit command



But that cannot model the Octal DDR SPI Serial NAND device's ODDR command sequence where the 1-byte command is received on **SIO[7:0]** pins and over ONE clock cycle

Also, note the use of the new **Data Strobe DS** signaling that cannot be checked in the older x4 SPI Serial NAND memory verification models

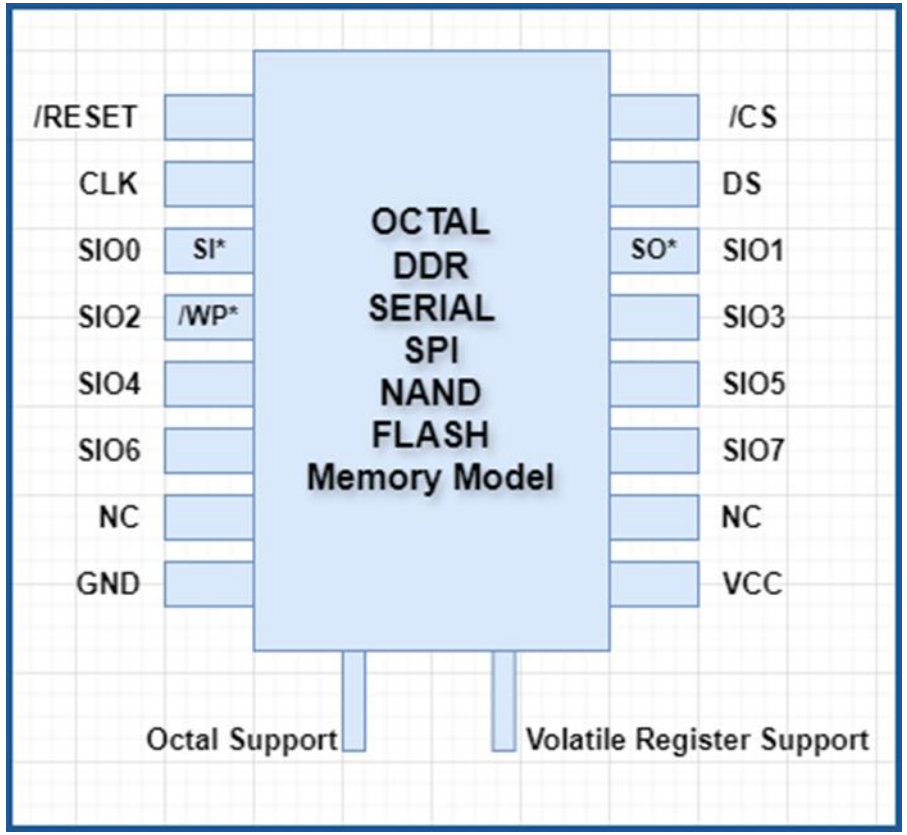


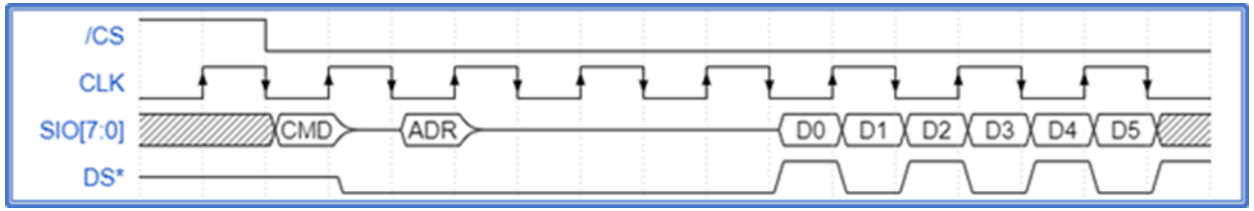
Solution

- Automotive SoC and Flash Controller Silicon IP developers require a proven and reliable solution for the recent SPI Octal DDR update to their controller
- Cadence, in partnership with Winbond a leading supplier of Octal Serial NAND in the automotive space, crafted a solution to add SPI Octal DDR Verification support
- The SPI Octal DDR NAND Flash Memory Model can offer up to the theoretical maximum 240MB/s continuous read data transfer rates at 120MHz simulation clock speeds
- New command specifications, as described in the Winbond datasheets, are supported in the SPI Octal DDR mode. The command format follows the C-A-D (Command-Address-Data) sequence as specified in the datasheets
- The Memory Model is fully backward compatible, as specified in the datasheets
- Depending on the configuration programmed by the user, the model can operate in 1-bit SPI Single Data Rate (SDR) mode, 1-bit SPI Double Data Rate (DDR) mode, 8-bit Octal SPI SDR mode, or 8-bit Octal SPI DDR mode

Implementation

- The Cadence SPI NAND Flash Memory Model now supports this new capability, which can be enabled in the Memory Model with a new configuration parameter
- There is an additional configuration parameter that enables the Memory Model support for a Volatile Configuration Register that allows programming the correct Octal transfer mode
- In this SPI Octal DDR mode, the legacy SI and SO pins are reused as SIO0 and SIO1, respectively, the /WP pin is reused as SIO2, and new SIO3-SIO7 pins are added to the package.
- There is also a new Data Strobe output pin, DS, that acts in conjunction with the read data to signal the host controller to latch data when running at the maximum DDR frequencies
- The SPI Octal DDR mode can be configured with or without DS (Data strobe); the DS-selection can be made via the Write Volatile Config Register command flow, as described in the datasheets
- With the SPI Octal DDR interface, the data transfers over the Serial NAND wires are adapted to utilize the 8-bit wide data bus now available, along with the data strobe transferring data on every clock edge





Implementation Details

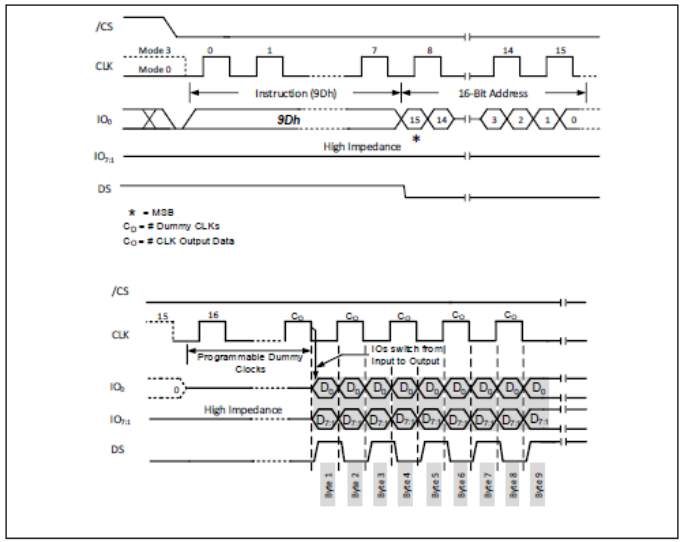


Figure 8-49 DDR Fast Read Instruction SDR mode (Buffer Read Mode, BUF=1)

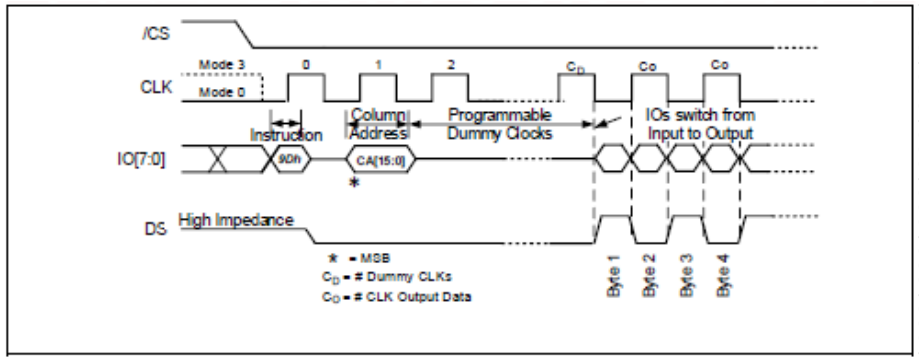
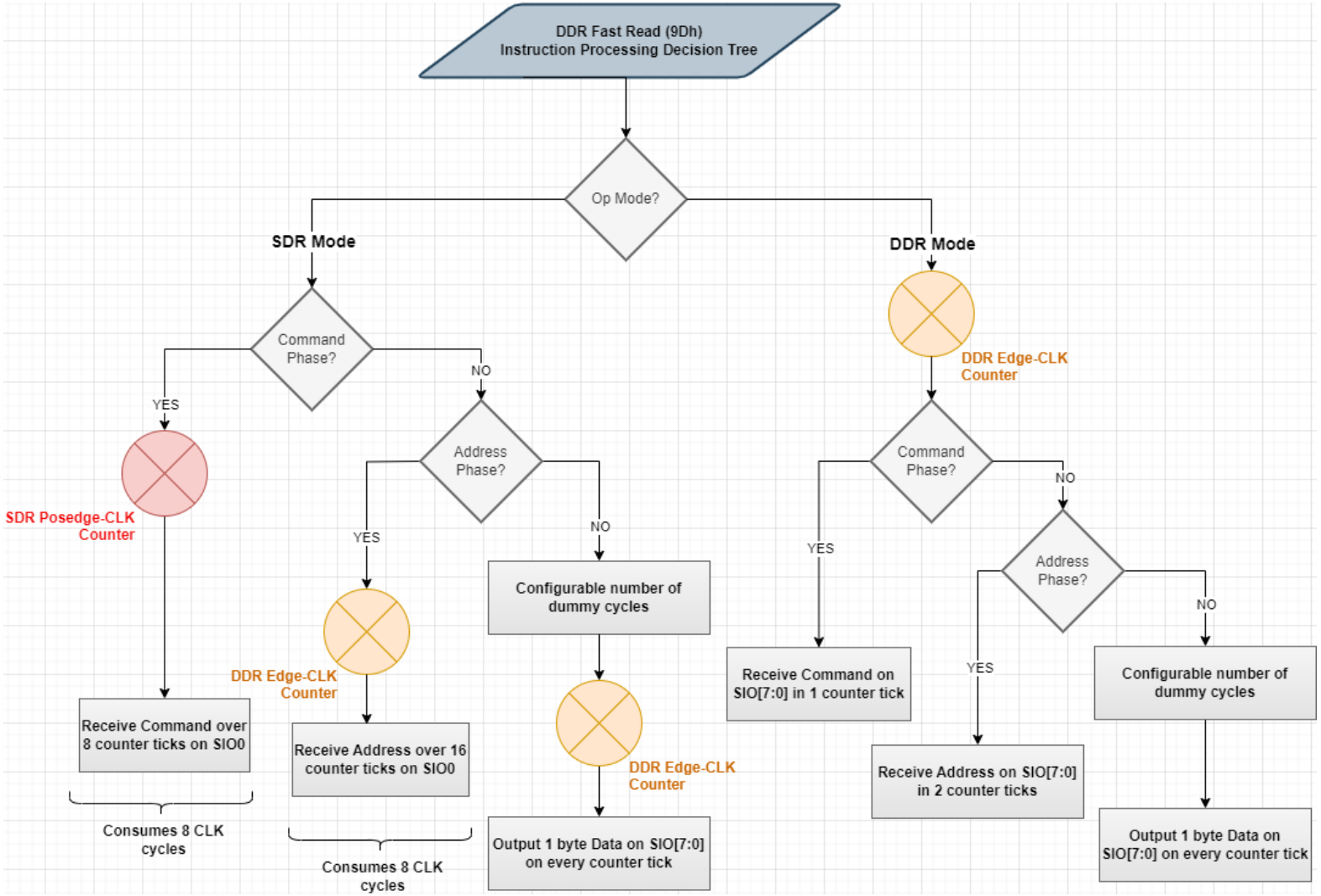


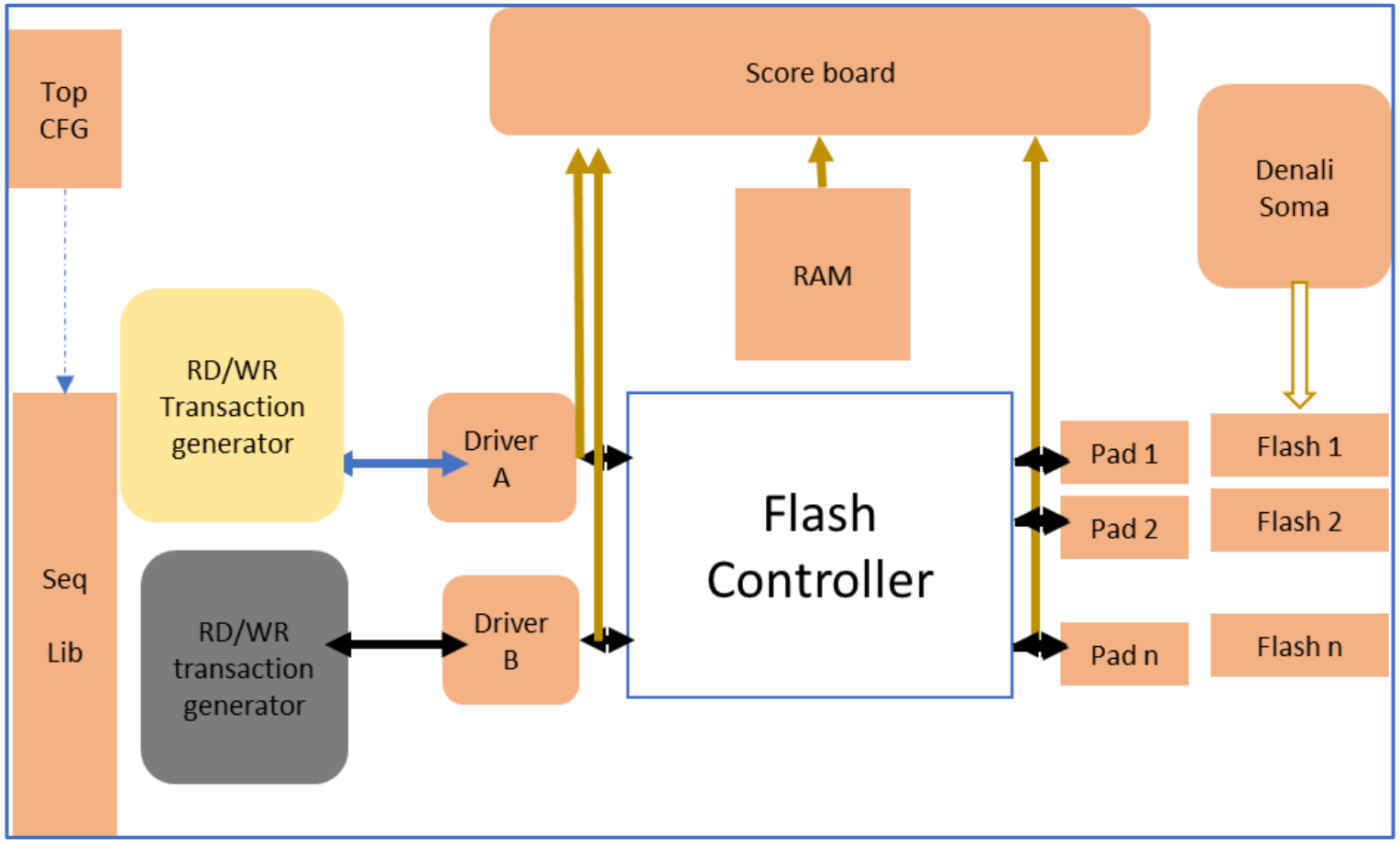
Figure 8-51 DDR Fast Read Instruction ODDR mode (Buffer Read Mode, BUF=1)

Source: Images from Winbond W35N01JW Datasheet



Summary of Results at NXP - 1

- Able to integrate SPI NAND Cadence VIP in test environment seamlessly
- Works for different density grades
- Command adapts as per current density grade



NXP Flash Controller testbench

Summary of Results at NXP - 2

- Extensive checks in VIP helps identifying bugs in Design IP for incorrect register configurations which require specific values for different range of frequencies
- Invalid data region based on Data Valid Window timer
- VIP drives valid data during valid window timer and drives X after window passes

```
*Denali* Error: Detected[testbench.flashA.flash] ADDR_NOT_COMPLETED @2503648596 ps :: For Fast Read Octal DDR Output Command command the CSn pin is de-asserted @ 2503648596 ps But the Address cycle is not completed.
*Denali* Error: Detected[testbench.flashA.flash] DUMMY_CYCLE_NOT_COMPLETED @2647085497 ps :: Dummy cycle not completed. CSn high without DataIn or DataOut for Fast Read Octal DDR Output Command command @ 2647085497 ps
```

```
*Denali* Error: Detected[testbench.flashA.flash] WRITE_ENABLE_OR_DISABLE_DURING_BUSY @521191345 ps :: Command Write Enable given during Read, Program or Erase busy period @ 521184681 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521551201 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521557865 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521564529 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
```

- Verify correct AC timings for Controller Design IP

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*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO5
*Denali* Error: Detected[testbench.flashA.flash] DATA_IN_HOLD_VIOLATION @453246701 ps :: Data In Hold Time violation of 200 ps @ 453246701 ps on SIO5 signal.

*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO6
*Denali* Error: Detected[testbench.flashA.flash] DATA_IN_HOLD_VIOLATION @453246701 ps :: Data In Hold Time violation of 200 ps @ 453246701 ps on SIO6 signal.

*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO7
```